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IRVINE

Three Dimensional Electromagnetic Field Simulation of Integrated Metal-Insulator-Metal Capacitors

THESIS

submitted in partial satisfaction of the requirements for the degree of

MASTER OF SCIENCE

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by

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1998

To my mom...

... ok, and to my sister

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Acknowledgments

I want to thank Professor G. P. Li for his academic guidance and assistance, but specially for his kindness. There is something beyond engineering and not everyone remembers.

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And of course to all those people who helped in some way during my research, even when it was by letting me forget about it for a while (go ahead, self-include yourself).

Assume high Q possition!

ABSTRACT OF THE THESIS

Three Dimensional Electromagnetic Field Simulation of

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by

Francisco J. Lopez-Dekker

University of California, Irvine, 1998

Professor G. P. Li, Chair

Novel Metal Insulator Metal (MIM) Capacitors are studied using traditional S-parameters measurements and a 3-D Electromagnetic Field Simulation Tool. The simulation tool allows us to study the fields induced in the device when operating at high frequencies. Being able to study the fields allows us to obtain a better understanding of the device's behavior.

The new MIM capacitors introduce an extra Titanium Nitrite layer, very close to the Metal-2 layer, to achieve a high capacitance per unit area. The upper capacitor plate is fingered to reduce the series resistance and the parasitic inductance.

Structures with different number of fingers are studied and compared. Multi-finger structures behave better at moderate frequencies, but present some problems at higher frequencies. The importance of optimizing the interface between the capacitor and the connecting microstrip is demonstrated.

It is shown that the 3-D electromagnetic field simulation tool tested, although with some accuracy problems, is a useful and valuable tool to evaluate and analyze integrated passive components for RF applications.

I. Introduction

Monolithic Microwave Integrated Circuits (MMIC) are microwave circuits in which active and passive components are implemented on the same semiconductor substrate. MMICs can work at frequencies ranging from 1 GHz up to well beyond 100 GHz. MMICs can be applied to mobile communication systems, military or civil radar systems, satellite communications, GPS systems…

Especially the rapidly growing wireless communication market has boosted the development of MMICs. For example, according to a rapport of CIBC Oppenheimer, the GaAs analog semiconductor market grew approximately 35% in 1997, reaching $1.35 billion.

Fully integrated MMICs compete against discrete element solutions. MMICs are clearly better when weight and size are a problem. Another definite advantage is their lower cost when mass-produced.

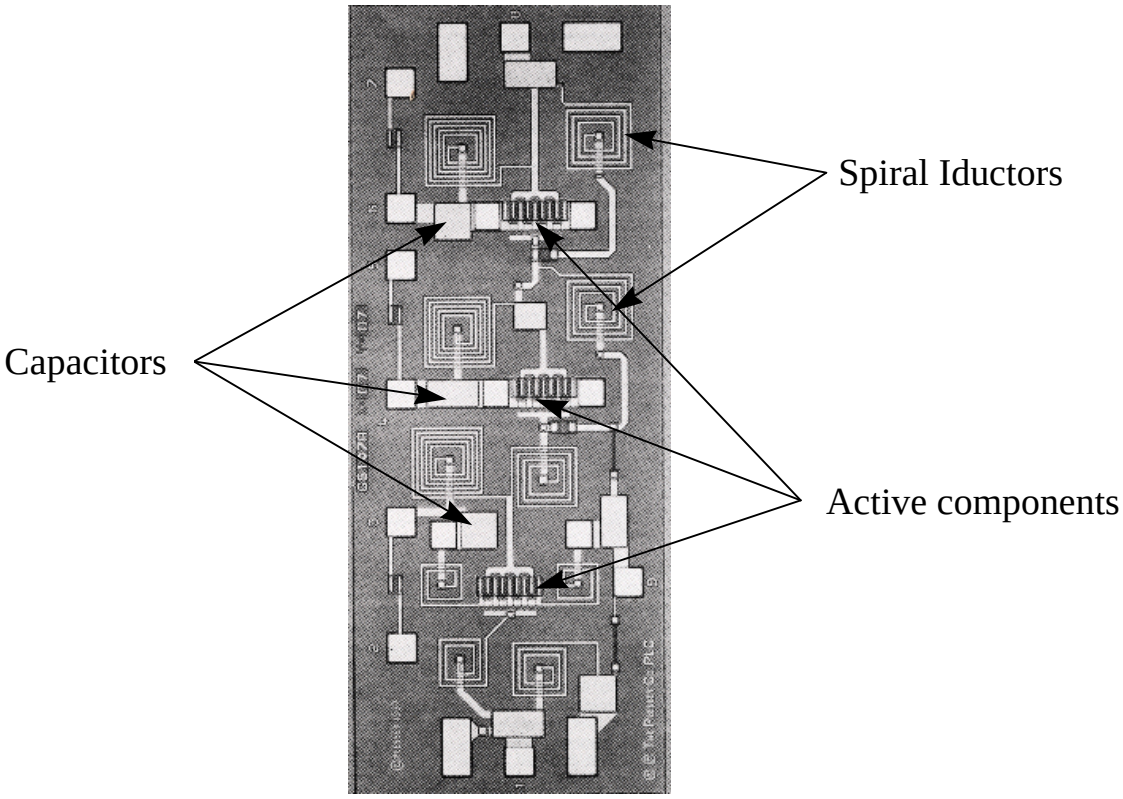

Figure I-1: An example of a three stage MMIC amplifier for a satellite receiver.

I.1 Passive components

As I mentioned above, MMICs integrate active and passive elements, in contrast to Hybrid Microwave Integrated Circuits (MICs) where lumped external passive components are often used. Examples of passive elements are spiral inductors (see Figure I-1) and Metal Insulator Metal (MIM) Capacitors.

Although passive elements, as capacitors, inductors and resistors, may seem rather simple when compared to active components, in reality it turns out that integrating them is a very challenging undertaking. An obvious example is the integration of

inductors. Lumped inductors are essentially three-dimensional structures, whereas all devices on integrated circuits have to be very planar. The most common planar inductor, the spiral inductor, is much more complicated than an external solenoidal inductor.

Thus, the planar nature of integrated circuits, and the limited availability of space makes the integration of a priori uncomplicated devices a difficult task.

The main requirements involved in designing integrated passive elements are:

1. To achieve a high Quality Factor. This is equivalent to keeping the parasitic elements (the parasitic inductance in resistors and capacitors; or the parasitic capacitance in inductors, etc) as small as possible. High Q Inductors and Capacitors are essential for narrow band circuits as filters.
2. Make reproducible devices. For narrow band applications the tolerance of the circuit elements has to be very small. For example, you could have a nearly ideal capacitor, but a small departure from the nominal capacitance could make the whole circuit useless.
3. Reduce the chip area needed for those devices. As illustrated in Figure I-1 inductors and capacitors tend to occupy most of the available chip area. Thinking in terms of a *system on a chip,* it is important to reduce the area needed to implement passive components to be able to fit the rest of the system.
4. Implement passive elements using *everyday* technology. It is possible to think of exotic designs that would result in small high quality devices, but they need to be

doable in practice, and doable at a reasonable cost. That means that passive element designs should be implemented using the available fabrication techniques and, when possible, without introducing any new processing steps.

I.2 MIM Capacitors

Recently a considerable amount of effort has been devoted to the study, characterization and development of inductors, especially spiral inductors [1]. However, little work has been done on Capacitors, probably because they have been considered to be less complicated and troublesome.

Nevertheless, capacitors are encountered in large quantities in RF circuitry. This fact alone makes them worth an in-depth analysis. Furthermore, their behavior turns out to be more complicated than expected and obtaining devices with a high quality that are small and have a reproducible capacitance is anything but straightforward.

There are several ways to fabricate capacitors in integrated circuits process. An attractive, alternative way, not covered in this paper, is interdigital capacitors. In our work we will concentrate on the study of certain kinds of MIM Capacitors on a lossy Silicon substrate. Progress in material processing has made silicon feasible for certain low power RF circuitry. However, the substrate has still greater losses than, for

example, GaAs substrate, adding extra constraints and limitations that have to be considered.

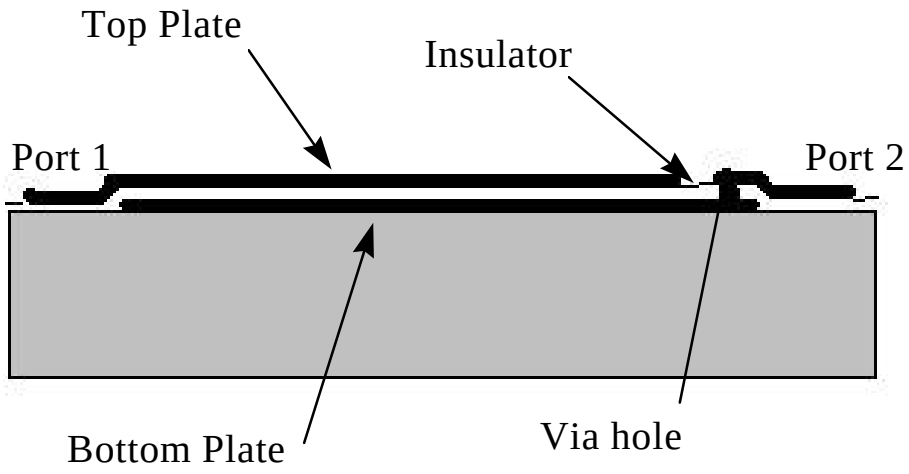

Figure I-2: Schematic view of a MIM Capacitor.

MIM Capacitors are a very intuitive way of implementing capacitors. A MIM Capacitor is basically a parallel plate capacitor as shown in Figure I-2. In the devices that we study the bottom plate will be in the Metal-2[1] layer. If Metal-3 was used for the upper plate, the separation between the plates would be too large to achieve an acceptable capacitance. Therefore we introduce an extra conducting layer, which in our case will be a layer of Titanium Nitrite.

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[1] In IC-process several metal layers are introduced. These layer are numbered from bottom to top. The layers are isolated by an oxide layer, an connected to each other or to the active components through via-holes.

In order to reduce the losses associated to the lossy silicon substrate, a thick oxide layer separates the substrate from the device.

To reduce the parasitic inductance and the series resistance we will study a fingered structure. By fingering the capacitor we also expect to gain some extra fringing capacitance.

I.3 3D Electromagnetic Field Simulation

Besides the study of the proposed MIM Capacitor themselves, one of the main purposes of this work is to experiment and validate a 3D Electromagnetic Field Simulation method to study integrated devices for RF applications.

Traditionally, RF devices are studied by measuring them, usually doing S-parameters measurements using a network analyzer. Ideally, if we were able to model the device accurately and to find an exact solution for the Maxwell Equations, we could study the device without having to do any measurement. In practice the devices are not easy to model and the equations involved are extremely difficult to solve.

Nevertheless, as the available computing power steadily increases, simulation tools are appearing as a valuable aid in the development of Integrated Circuits. This is because the simulation offers the following features or capabilities:

1. It is fast in the sense that a new device or a modified device can be tested right away. To do measurements the structure has to be implemented in a test chip and that requires, in general, more time.
2. It allows the designer to test and model devices that cannot be (yet) manufactured. This can serve as a first test before actually modifying the fabrication process to implement the device. It also can be of use to model devices that cannot be fabricated at all, but that are still of interest.
3. It allows design engineers to study the devices in new ways, to look at things that cannot be measured. In our case, we will demonstrate the utility of studying the Electromagnetic fields induced by the device. By gaining access to this new source of information the device subjected to study can be better understood, problems can be identified directly, and solutions for these problems can be tested and validated.

Performing 3D Electromagnetic Field simulation is still a computationally expensive procedure. There are other options, like 2.5D simulation techniques, and for some purposes those can be valid and even optimal methods. However, we believe that as the frequency goes up, and structures become more and more complicated, the full 3D Simulation method is preferable.

I.4 Organization of this Thesis

Chapter II will describe the simulation methodology used in our work. The simulation process will be detailed and validation techniques will be introduced.

In Chapter III the MIM Capacitors that have been studied and used to experiment with the simulation technique will be presented and described.

In Chapter IV we illustrate and explain the measurement results on these MIM Capacitors. Besides these measurements, we will compare them to the simulation results in order to test and validate the simulation process.

Chapter V presents a qualitative analysis of the Electromagnetic Fields associated to our devices.

Finally, in chapter VI the conclusions and suggest some ideas for future research will be presented.

II. Simulation Methodology

As explained in the previous chapter, simulation not only allows us to study devices without having to implement them, thus saving development time and costs, but also enables us to study features that are very difficult or impossible to measure. This can be very helpful to understand the behavior of the device. However, a drawback of the simulation is that it cannot include *all* the effects encountered in reality, hence limiting the accuracy of the simulation results. Any algorithm we can use will introduce some inherent limitations as to what can be simulated.

In our case, the simulation software used, *Ansoft*'s HFSS, cannot model semiconductors in the sense of having minority and majority carriers, diffusion currents, etc. It also cannot model certain geometries with precision.

Another source for errors is the numerical nature of the solution found by the simulator. Although the numerical error can be, theoretically, made as small as

desired, in practice we encounter severe computational limitations: limited available memory and limited computation time. We can reduce the computational load of the problem by simplifying the simulated model. Although this itself is a source of error, it is essential to get meaningful results.

The existence of these sources of error introduces the need to validate the results. To do this we have to compare simulated data to measured data. In case both results do not agree we have to refine the simulation. We can and should learn from the cases in which we have measured results, so that we can rely on the simulation in those cases when we do not have measurement results of the actual device.

II.1 The Simulation Process

Figure II-1 shows the flowchart describing the complete simulation process. The process starts with a physical description of the device we are characterizing. This description is divided in two parts:

1. A layout file that describes the geometry of the device. A typical format for this file is the GDSII format.
2. A set of process specification containing the thickness of the different layers, the characteristics of the materials for each layer, etc.

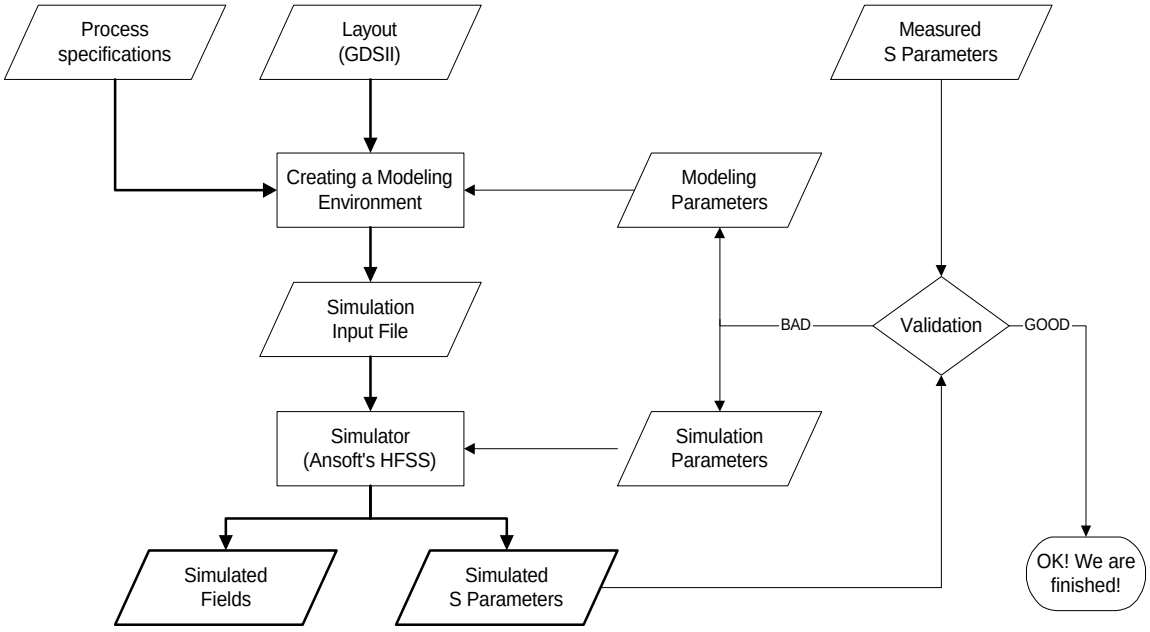


Figure II-1: Flowchart of the simulation process. The process is pseudo-iterative, since the number of iterations should be reduced to one when the process is tuned.

We use this physical description to create a modeling environment. We explain this sub-process in detail in section II.2. The result of this process is a 3-dimensional model for which the Maxwell Equations can be solved by HFSS.

The next step in our process is the actual simulation using HFSS, controlled by a set of simulation parameters that determine some computational aspects of the solution. The simulator has the following outputs:

1. The EM field solutions for the simulated 3D space at a given frequency.
2. A set of scattering parameters for the simulated device.

If we are simulating a device for which we do not have any measurement results, the process almost ends at this stage. The obtained scattering parameters are not those for the device but those for the entire model we have simulated. As with real measurements we have to connect the device to the *outside world* in order to feed a signal into the system. Section II-3 describes the process of de-embedding our device's scattering parameters.

However, if we dispose of measurement results we can, or rather have to, use them to validate the simulation. This is done simply by comparison of the de-embedded simulated parameters with the measured parameters. In case both results do not agree we have to either change some modeling parameters or some computational simulation parameters.

In some cases, inaccuracies inherent to the simulation and, especially, those caused by limitations to our computational power, make it unrealistic to for exact numerical answers. This is a common situation because the full 3-D electromagnetic field simulation places very high requirements on the computing resources. In those cases, we are bound to look for qualitative trends in the frequency domain. Hence, the validation step becomes a rather subjective step to be done by the engineer.

II.2 Creating a Modeling Environment

One of the most critical steps in the simulation process is the creation of the model that we are going to simulate. In this section we treat this step in detail. The objective of this step is to create a modeling environment containing the device we are studying. Several factors have to be taken into account when creating this model. Some of these factors are the consequence of explicit restrictions of the simulation software; the most important of these restrictions is that not all materials we encounter can be modeled. For example, we cannot implement, at this point, semi-conducting materials. However we can try to find an alternative that behaves as close as possible.

However, most of the limitations are a consequence of the finite computational power we have. There are several techniques to reduce the computational load of the simulation, but each technique has its drawback:

1. The size of the simulated 3-dimensional space containing the device has to be made as small as possible. By doing so we reduce the number of nodes in the finite element solution, but we are approaching artificial boundaries that will distort the result of the simulation.
2. The number of different objects we create has to be kept small. The only way of doing so is by eliminating some (superfluous) elements in our device. For example, in our simulations of MIM Capacitors we have ignored the Metal 4 and Metal 5 layers, since they were only used to interconnect the device to the outside world.

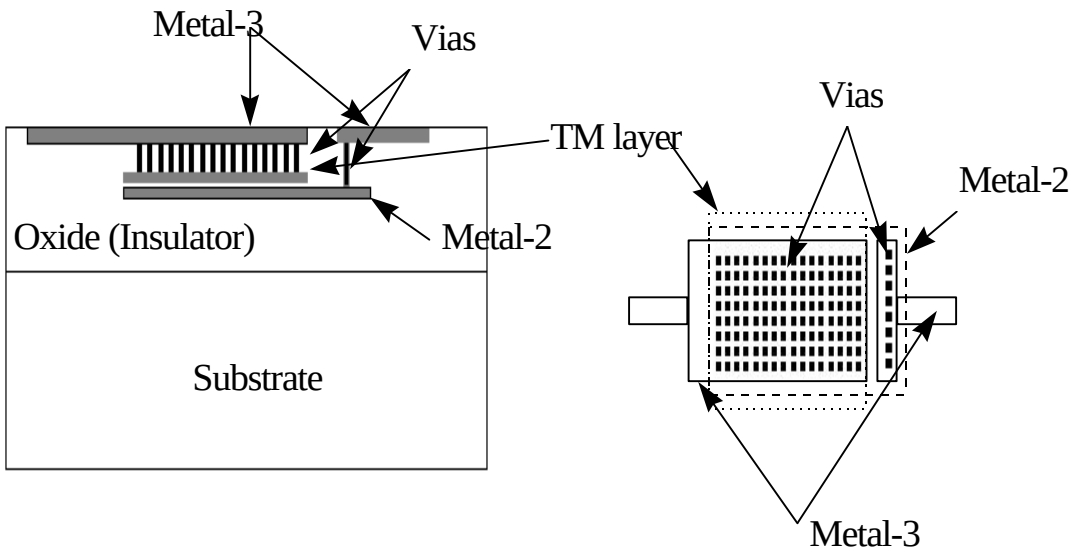


Figure II-2: Schematic model of a MIM Capacitor. Left: Cross section. Right: Layout. Metal 3 is connected to the TM layer through an array of via holes. Notice the large number of via, which therefore would be difficult to model.

1. We have to pay special attention to via holes (see Figure II-2). In some cases in our IC design we encounter that different metal levels are interconnected with arrays of via holes, needed to obtain a low resistance interconnection. Modeling each via hole independently would imply having hundreds of tiny objects making the overall model much more complex. It is convenient to replace this array of via holes by an equivalent model. For an array of N via holes, each having an impedance $R_{via,}$ occupying an area $A_{via,}$, if the distance between the interconnected metal levels is d, we can find a material with an *equivalent* conductivity

$$s_{eq} = \frac{N \cdot d}{R_{via} \cdot A_{via}} \qquad \text{(II-1)}$$

Of course this is not an exact equivalent. For example, a material with this equivalent conductivity would allow horizontal current, whereas clearly the via holes only allow vertical currents.

Figure II-3 shows a flowchart of the process followed to create the modeling environment. As shown, the first step is to convert the layout to a format that can be

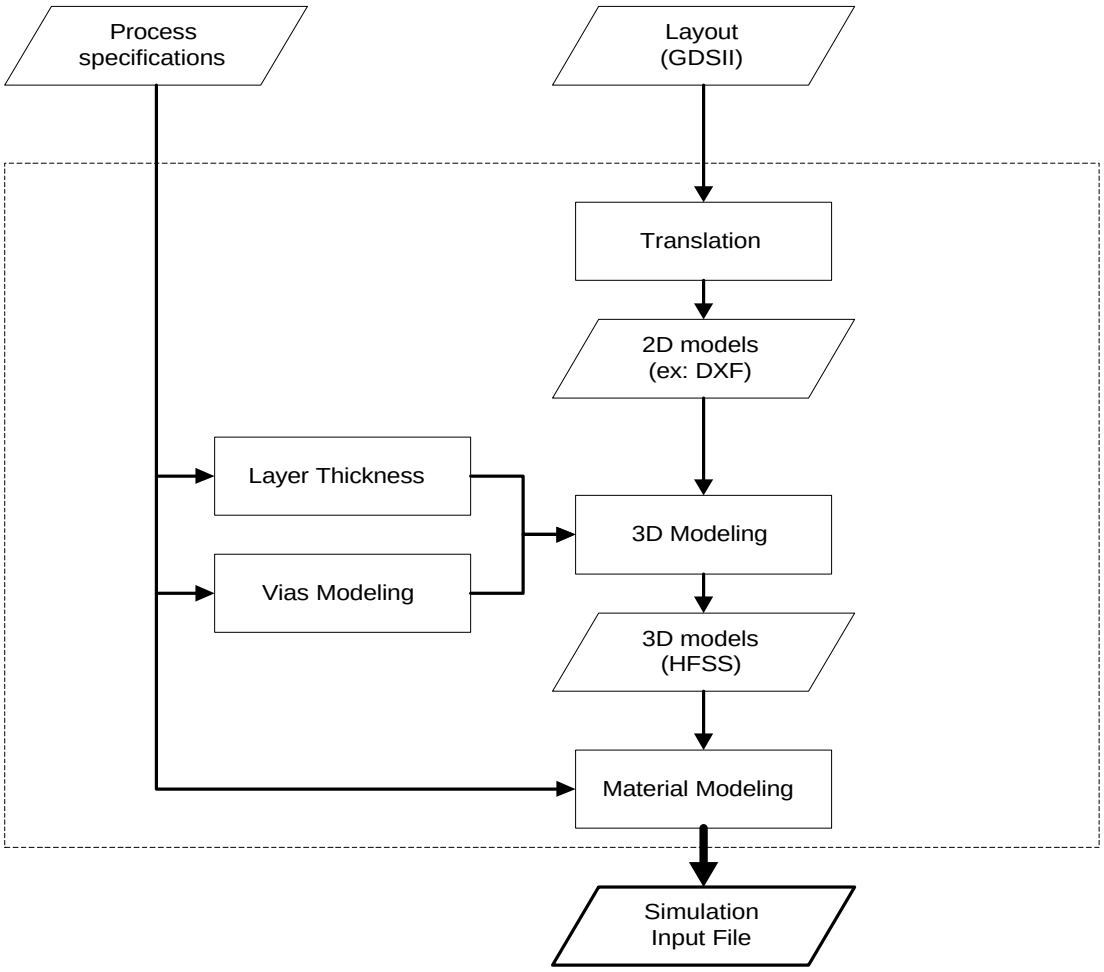


Figure II-3: Flowchart describing the sub-process in which the modeling environment is created.

read by HFSS. We can do this using commercial software packages or we can do it manually. Once we have the 2-dimensional models the thickness of each layer is extracted from the process specifications to create 3D models. The last step is to assign material properties to each object. In this last step via hole connections are approximated as explained earlier and semi-conducting materials are modeled as materials with the corresponding conductivity.

II.3 De-embedding Parameters

As mentioned earlier, we do not simulate only the device under study. In addition to the device, we have to model the microstrip lines connecting it to the outside world. Also, a signal has to be fed into the system through a port. It is very difficult to obtain a perfect matching between the port and the microstrip line. Furthermore, the line itself has some effect on the result of the simulation. We have to cancel out all these undesired contributions when characterizing our device, very much as in *real world* measurements.

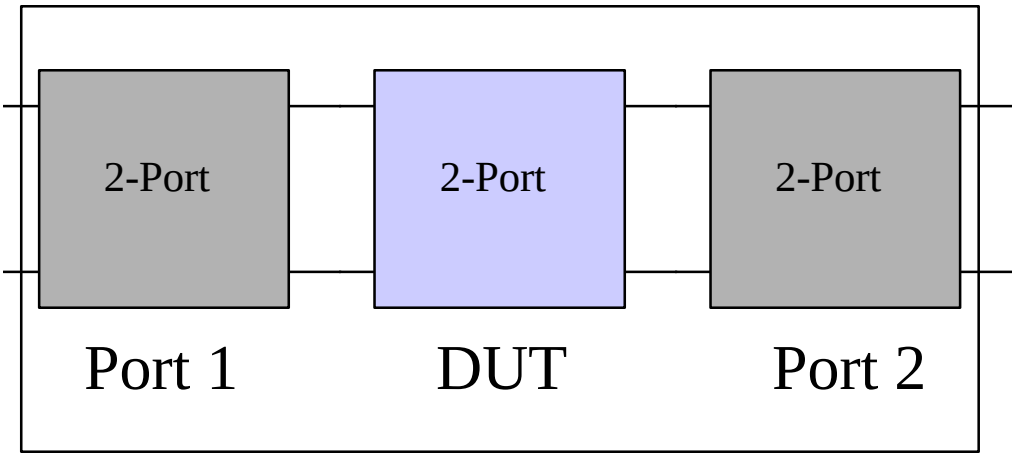


Figure II-4: A cascade of 2-Ports representing real measurement or simulation conditions. The effect of the input and output stage has to be eliminated.

Figure II-4 represents this situation. It is shown how we are measuring a cascade of three 2-Ports, where the middle one corresponds to our device.

This kind of structures is easier to handle using the *ABCD*-Parameter Representation [2]. The *ABCD*-Parameters relate voltage and current on one port with voltage and current on the other port:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \cdot \begin{bmatrix} V_2 \\ I_2 \end{bmatrix}$$

(II-2)

ABCD-Parameters can be easily calculated from S-Parameters and vice-versa using the following expressions:

$$A = \frac{(1+S_{11})(1-S_{22})+S_{12}\cdot S_{21}}{2\cdot S_{21}} \quad B = \frac{(1+S_{11})(1+S_{22})-S_{12}\cdot S_{21}}{2\cdot S_{21}}$$
$$C = \frac{(1-S_{11})(1-S_{22})-S_{12}\cdot S_{21}}{2\cdot S_{21}} \quad D = \frac{(1-S_{11})(1+S_{22})+S_{12}\cdot S_{21}}{2\cdot S_{21}} \qquad \text{(II-3)}$$

And:

$$S_{11} = \frac{A+B-C-D}{A+B+C+D} \quad S_{12} = \frac{2\cdot(A\cdot D-B\cdot C)}{A+B+C+D}$$
$$S_{21} = \frac{2}{A+B+C+D} \quad S_{22} = \frac{-A+B-C+D}{A+B+C+D} \qquad \text{(II-4)}$$

To obtain the *ABCD*-Parameters for the cascade of three 2-Ports, we simply have to multiply the individual matrixes:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \cdot \begin{bmatrix} A_{dut} & B_{dut} \\ C_{dut} & D_{dut} \end{bmatrix} \cdot \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \qquad \text{(I-5)}$$

Starting with S-Parameters it is easy to see that if we take Port 1 and Port 2 in Figure II-4 to be symmetric, then:

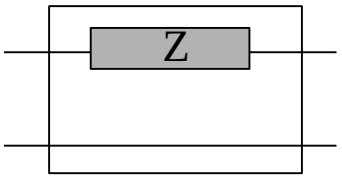
$$\begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} = \begin{bmatrix} D_1 & B_1 \\ C_1 & A_1 \end{bmatrix} \qquad \text{(II-6)}$$

Now, to find the parameters corresponding to the device itself we can use the expression:

$$\begin{bmatrix} A_{dut} & B_{dut} \\ C_{dut} & D_{dut} \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix}^{-1} \cdot \begin{bmatrix} A & B \\ C & D \end{bmatrix} \cdot \begin{bmatrix} D_1 & B_1 \\ C_1 & A_1 \end{bmatrix}^{-1} \qquad \text{(II-7)}$$

Now the only thing remaining is to find the values for A_1, B_1, C_1 and D_1. There are a couple of additional properties of the *ABCD*-Parameters that make this task easier:

1. *ABCD* matrix for an impedance:



$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} 1 & Z \\ 0 & 1 \end{bmatrix}$$

2. If the network is reciprocal:

$$A \cdot D - B \cdot C = 1$$

Now, if instead of having an unknown device we put a 2-port, as in property 1, with a known impedance, equation II-5 gives us a set of four equations. Out of these four only three are independent:

$$\left.\begin{aligned} A &= A_1 \cdot D_1 + B_1 \cdot C_1 + A_1 \cdot C_1 \cdot Z \\ B &= 2 \cdot A_1 \cdot B_1 + A_1^2 \cdot Z \\ C &= 2 \cdot C_1 \cdot D_1 + C_1^2 \cdot Z \end{aligned}\right\} \qquad \text{(II-8)}$$

In these equations the left-hand term is a simulation result (or a measured result), and the right hand term is dependent on the *ABCD* matrix of the port. Using two different known impedances we get an over-determined set of equations that can be rewritten as an optimization problem, where the function to be minimized is of the form

$$f(A,B,C,D) = \left|A_I - A_1 \cdot D_1 - B_1 \cdot C_1 - A_1 \cdot C_1 \cdot Z_I\right|^2 + ... + \left|C_{II} - 2 \cdot C_1 \cdot D_1 - C_1^2 \cdot Z_I\right|^2 \quad \text{(II-9)}$$

Note that *A, B, C* and *D* are complex variables. There are several efficient ways to solve this kind of optimization problems. For our purpose we have chosen to implement the Fletcher-Reeves Conjugate Gradients Method [3] (see implementation in Appendix 2).

Any pair of impedance would be appropriate. In our work we have chosen to use a zero impedance meaning that we have a “through” from port-1 to port-2, and a known resistor in the order of magnitude of Z_o, the characteristic impedance of the microstrip line used to connect our device. We choose to do this because a "through" and resistors are relatively easy to simulate.

II.4 Equivalent Capacitance and Quality Factor.

In our work we are dealing with passive elements, in particular with MIM (Metal Insulator Metal) Capacitors. Although we are interested in a detailed equivalent circuit for each device (figure II-5), in many cases it is sufficient or convenient to deal with an Equivalent Capacitance. When doing so we are assuming that we can model the device as in figure II-4, implying that there are no parasitic elements

connecting the device to the substrate (ground). All other parasitic elements can be included in Z. From Z we can calculate the admittance **Y** and the Quality Factor **Q** using:

$$Z = R + j \cdot X \Rightarrow Y = \frac{1}{R + j \cdot X}$$
$$Q = \frac{\mathrm{Im}(Y)}{\mathrm{Re}(Y)} \qquad \text{(II-10)}$$

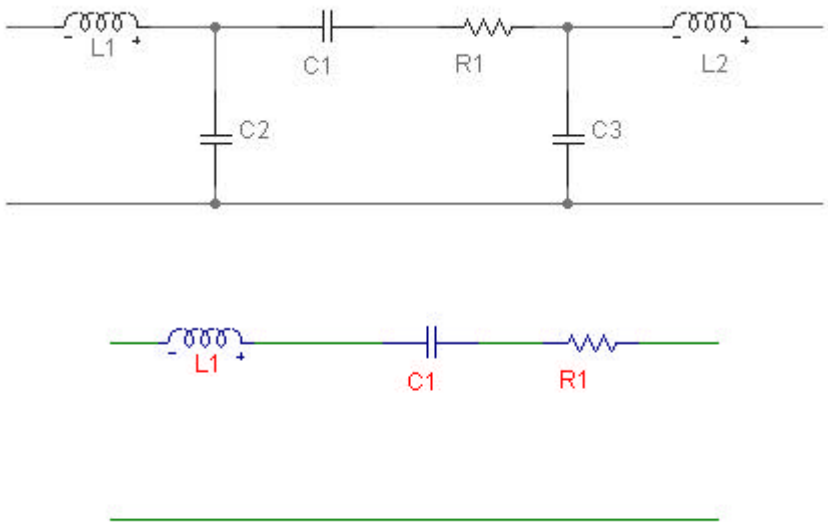


Figure II-5: Capacitor as a 2-Port. Top: Complete model. Bottom: Simplified RCL model assuming C_2 and C_3 equal to zero

Assuming that the imaginary part is only due to a capacitance, we can calculate the value of this equivalent capacitance $\hat{C}$ using:

$$\hat{C} = \frac{1}{w \cdot \mathrm{Im}(Z)} \approx \frac{C}{1 - L \cdot C \cdot w^2} \qquad \text{(II-11)}$$

where the last term represents the equivalent capacitance we obtain in case we only have a parasitic inductance in series with the capacitor (Figure II-5, bottom), which in many cases is a good approximation to reality.

III. MIM Capacitors: Description of the devices under study

As mentioned in previous sections, in this project we concentrate on the study of MIM (Metal Insulator Metal) Capacitors. There are various reasons to study this type of devices. First, these devices are a good frame to test and validate our simulation tool as a valid tool to help engineers in the development of new or better integrated (passive) components for high frequency applications.

Second, the devices themselves constitute a challenging field of study. So far little has been done to fully understand and characterize these devices, partially because they might be thought to be relatively simple. At this moment the increasing demand for integrated circuits for RF applications has resulted in a need to develop capacitors that combine a high quality factor with occupying the least chip area possible.

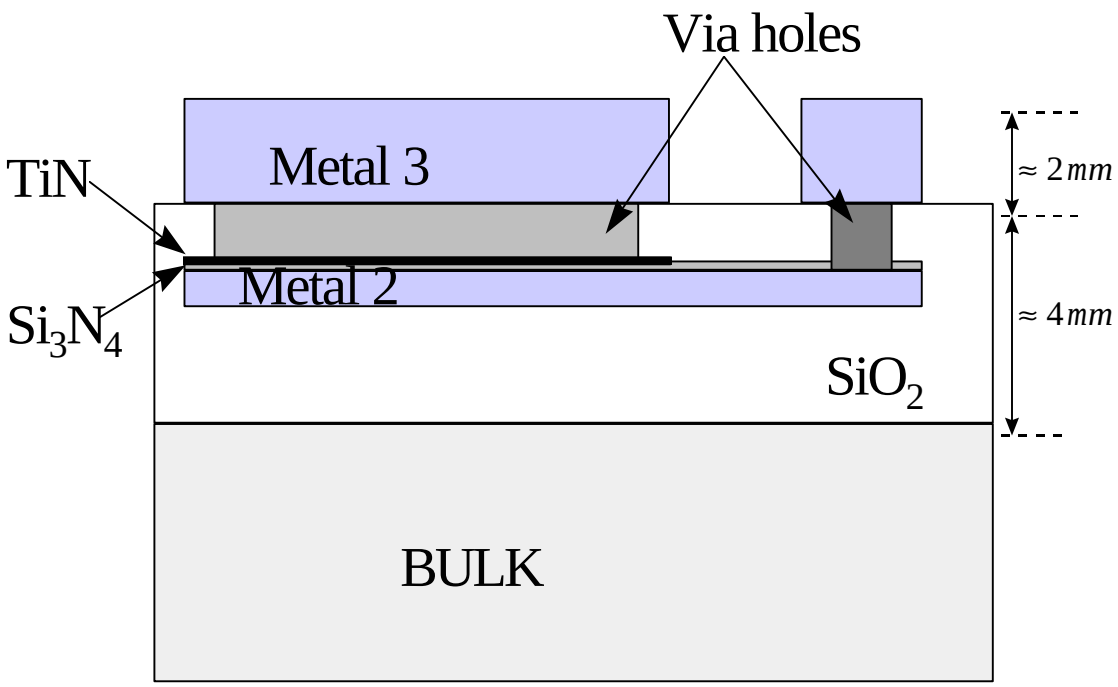


Figure III-1: Schematic cross section of the MIM Capacitors studied. A Parallel plate capacitor is formed between the Titanium Nitrate layer and Metal-2. A thick oxide layer isolates the bulk.

III.1 General structure of the MIM Capacitors under study.

Figure III-1 shows a schematic cross-sectional view of the MIM capacitors, as simulated, under consideration. The capacitor is a traditional parallel plate capacitor. Metal 2 is used for the bottom plate. To achieve a high capacitance we need to place the upper plate as close as possible to the lower plate, for this purpose an extra conductive layer is introduced between Metal 2 and Metal 3. This extra layer, the so-called TM ("Top Metal") layer, is a very thin (about 0.15µm) TiN Layer. The TM

Name	Thickness (μm)	ε_r	σ (S/m)	Masked	Comments
Metal 3	2.1	--	$3.1 \cdot 10^7$	Yes	Aluminum
Oxide 2	1	3.8	0	No	
Via 2a	0.8	4	$3.1 \cdot 10^4$	Yes	Connects Metal 2 to TM
Via 2b	1	4	$1.6 \cdot 10^6$	Yes	Connects Metal 2 to Metal 3
TM	0.15	--	$5.5 \cdot 10^5$	Yes	Capacitor Top Plate
Si_3N_4 layer	0.06	6.8	0	No	Capacitor Insulator
Metal 2	0.65	--	$3.1 \cdot 10^7$	Yes	Capacitor Lower Plate
Oxide 1	3	3.8	0	No	Isolation from substrate
Bulk	≥300	12	≈0.12	No	Modeled as a loosy dielectric

Table III-1: Principal process characteristics of the modeled devices.

upper plate and the lower Metal 2 plate are separated by a Si_3N_4 film, about 6 μm in thickness, as dielectric. Metal 3 presents a replica of the upper plate connected to it with a dense array of via holes to reduce the series resistance [4] of the device. In our simulated model we ignore the Metal 4 and Metal 5 layers, although the real implementation of the test devices uses those layers to achieve a low resistance connection to the *outside world*.

Table III-1 shows the most important characteristics of each layer. The values chosen correspond to those used in the simulation, which may differ slightly from the real case. Table III-1 indicates whether the layer corresponds to a layout mask. Oxide layers do not correspond to any mask.

Arrays of via holes can be modeled as conducting areas with a certain dielectric constant. The conductivity for these layers depends on the via-hole density. Modeling via holes in this way is not accurate mainly because it allows a horizontal current density. However, this will have small effect because of the high conductivity of the metal layers: horizontal currents will occur almost exclusively in those metal layers, while vertical currents will occur in the modeled via holes zone despite its low conductivity because it is the only way to lower layers.

III.2 MIM layouts

In our work we have been studying a series of different layouts. These layouts have a fingered upper plate as shown in Figure III-2. Between each upper plate finger, a narrow metal path is added that is connected through via holes to the lower plate (see Figure III-2). The five structures considered, named MIM1, MIM2, MIM3, MIM4 and MIM5 have respectively 1, 2, 4, 8 and 16 upper plate fingers. In all cases the upper plate area has been kept constant and equal to 160 μm^2, which with the data encountered in Table III-1 accounts for a nominal capacitance of 1.6 pF.

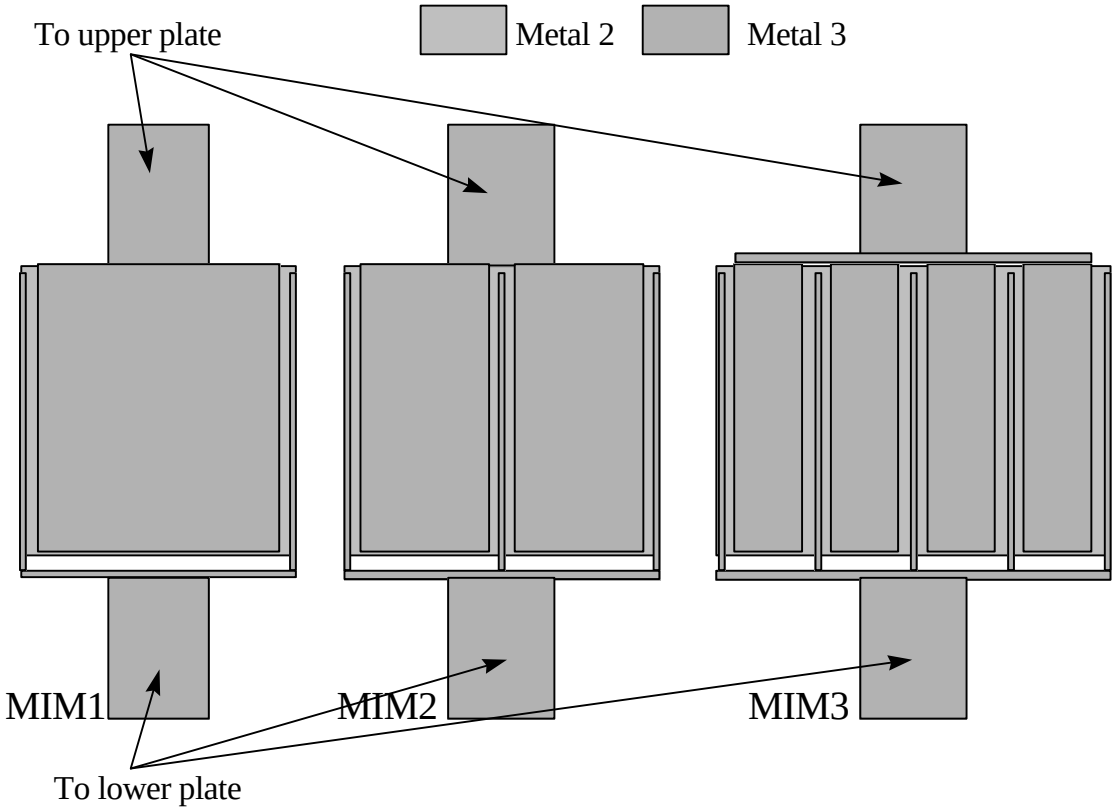


Figure III-2: Schematic layout of the MIM1, MIM2 and MIM3 Capacitors. The Metal-2 plates are connected to exactly equal TiN plates that serve as upper capacitor plates.

There are several reasons to experiment with these structures. The fingered structure results in a larger perimeter. It should be expected that it results in an increased capacitance due to more fringing fields. In [5] we find an approximate formula for the capacitance of a finite plate over an infinite ground plane:

$$C_{aprox} = \varepsilon_{ox} \cdot \left[1.15 \cdot \frac{(\text{plate area})}{H} + 1.4 \cdot \left(\frac{T}{H} \right)^{0.222} \cdot (\text{plate perimeter}) + 4.12 \cdot H \left(\frac{T}{H} \right)^{0.728} \right] \quad \text{(III-1)}$$

T is the thickness of the plate and H the distance between both plates. Although this formula is not accurate for the given dimension ratios, it can give us an idea of what should be expected. The second term gives us the fringing capacitance. Notice that in theory a capacitor could be designed for which the fringing capacitance would constitute the main contribution to the total capacitance. This could be done by shaping the upper plate in a way that it had a very large perimeter, for example, by having an extreme large number of very narrow fingers. Applying this formula to our layouts indicates that we could expect an additional capacitance of

$$\Delta C = 0.008 \cdot N \cdot pF \qquad \text{(II-2)}$$

where N is the number of fingers.

This predicts a decrease of capacitance per unit area because of the increase of the area needed to accommodate the multiple fingers while keeping the upper plate area constant.

IV. Measured Results and Validation of the Simulations on MIM Capacitors

In this section some measurement results will be presented which will be compared to simulation results in order to validate the simulation process. The devices tested are those MIM capacitors described in the previous section.

The measurements have been done using a Hewlett-Packard HP8510 Network Analyzer. The MIM capacitors are located in a test chip furnished by Rockwell Semiconductor Systems in a standard Ground-Signal-Ground configuration. The ground paths are also connected to the substrate.

IV.1 A reference

Before presenting our measured results, Figure IV-1 shows a plot extracted from [4]. This plot shows the equivalent capacitance and the quality factor as defined in Equation II-11 as a function of frequency for a set of MIM capacitors that are similar in structure to ours. In this plot different lines correspond to capacitors with the same

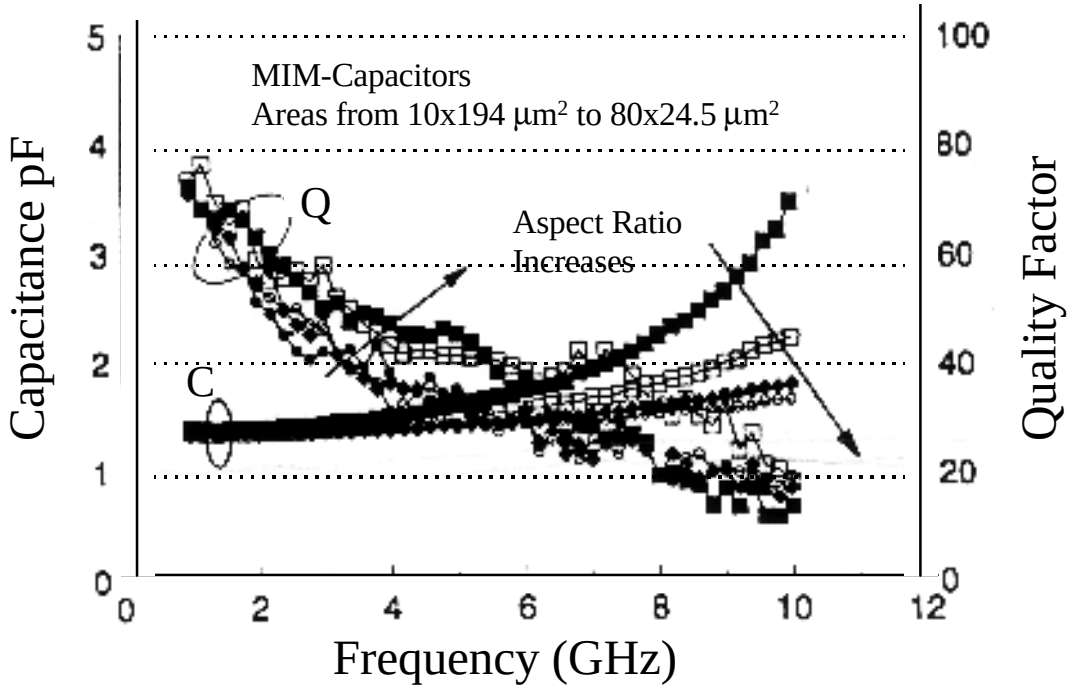


Figure IV-1: Published Capacitance and Q-factors for MIM Capacitors [4].

plate area but different aspect ratios. We will use these results as a reference and for comparison with ours.

This plot has several features we should emphasize:

1. The Quality factor decreases with frequency. This is because while the imaginary part decreases with frequency, the real part remains basically constant.
2. The dependence of the Q factor on the aspect ratio is weak.
3. The equivalent Capacitance increases with frequency. As in equation I-11 this should be attributed to a parasitic inductance.

4. The behavior of the capacitance is strongly dependent on the geometry of the device. When trying to explain this effect one should keep in mind that the test structure includes a piece of line connecting the device to the probe.

IV.2 Measuring Results

Figures IV-2 and IV-3 show respectively the capacitance and the quality in a frequency range of 50 MHz to 11 GHz.

Again we see how the equivalent capacitance rises (see Equation II-11) with frequency as a result of a parasitic inductance. There is not a clear trend in the effect of the number of fingers on the parasitic inductance

The behavior of the Quality factor is interesting in the sense that the effect of having more fingers changes as we go from lower to higher frequencies. At low frequencies multi-fingered structures show a better quality factor. A possible cause is a decrease in the series resistance of the connection to the bottom plate, due to multiple paths connecting it. But even at low frequencies the structure with 16 fingers is worse than the 8-finger one. At higher frequencies the 2 and 4-finger structures behave the best. We will try to give an explanation to this in later sections.

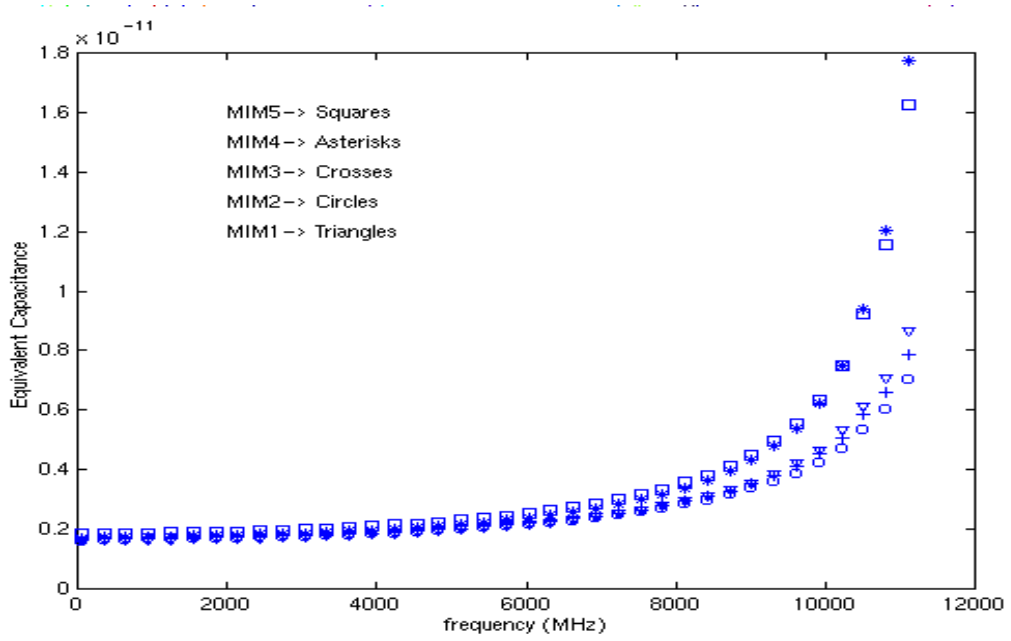


Figure IV-2: Equivalent Capacitance calculated from the S-Parameters for the five devices under test. The Equivalent Capacitance goes up as consequence of the parasitic inductance.

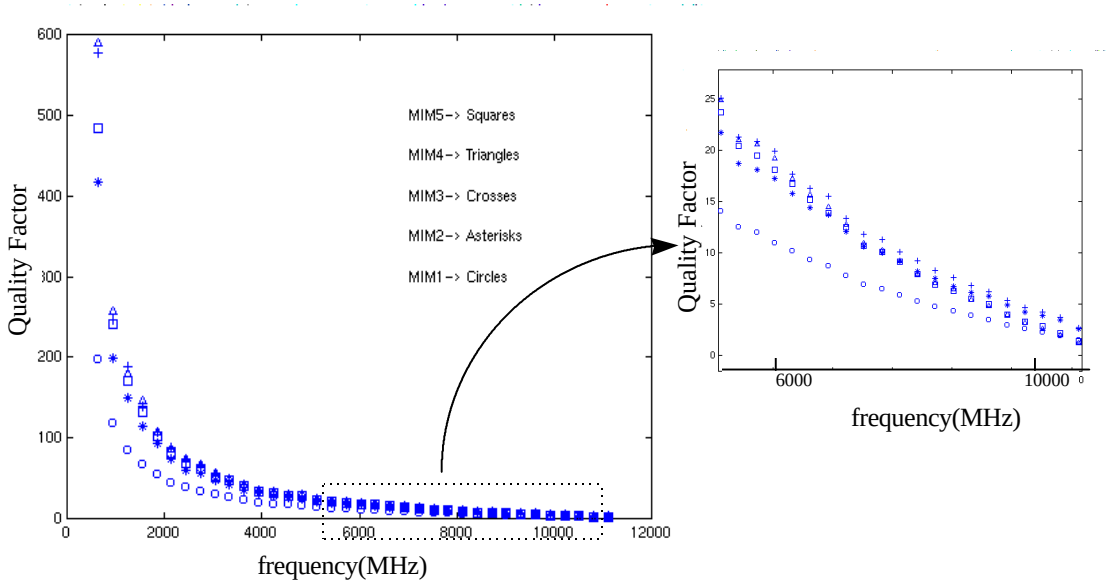


Figure IV-3: Quality factor of the devices under test vs. frequency. By zooming in we appreciate how different curves cross.

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We can model the capacitor by a **RCL** circuit and extract from the data the values of the series resistance, the capacitance and the inductance. The resistance has a DC component, R_{DC}, and an AC component, R_{AC}, linearly dependent on the square root of frequency [4] due to the Skin Effect [6]. Table III-1 shows these computed values.

Fingers	C (ρF)	L (ρH)	R_{DC} (Ω)	R_{AC} $f^{-1/2}$ (Ω $Hz^{-1/2}$)
1	1.646	101	0.79	$0.37 \cdot 10^{-5}$
2	1.649	96	0.40	$0.39 \cdot 10^{-5}$
4	1.677	97	0.30	$0.38 \cdot 10^{-5}$
8	1.733	106	0.27	$0.39 \cdot 10^{-5}$
16	1.849	99	0.30	$0.35 \cdot 10^{-5}$

Table IV-1: Principal characteristics extracted from the measurements on multi fingered MIM Capacitors

We observe that the number of fingers largely affects the DC series resistance, but we observe that while adding fingers to a small existing quantity has a large positive effect on it. As the number of fingers increases this effect becomes smaller and even negative. The parasitic inductance and the AC resistance are practically structure independent. This suggests that in both cases most of it can be attributed to the line

connecting the device to the micro-probe and eventually to the network analyzer. Structure dependencies are hidden behind this constant value.

Figure IV-4 and Figure IV-5 plot the capacitance and the capacitance per chip area vs. the number of fingers.

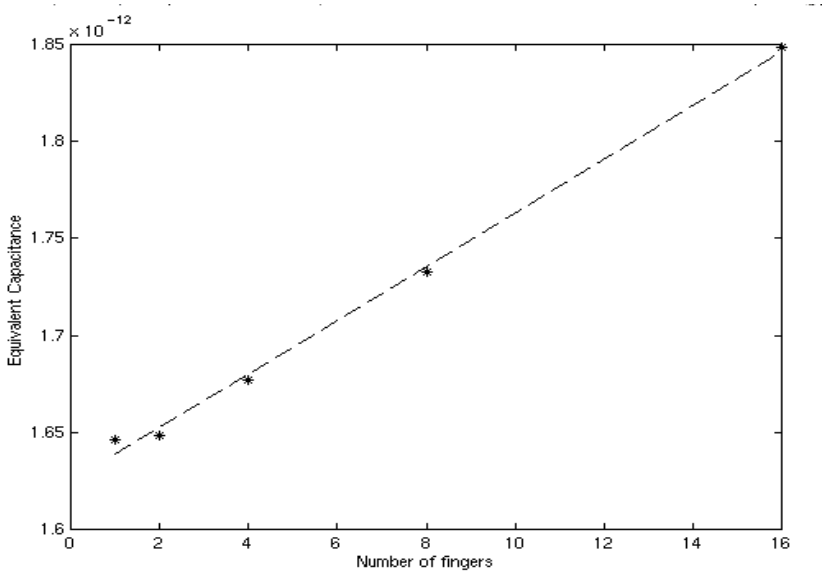

Figure IV-4: Capacitance Vs. Number of fingers.

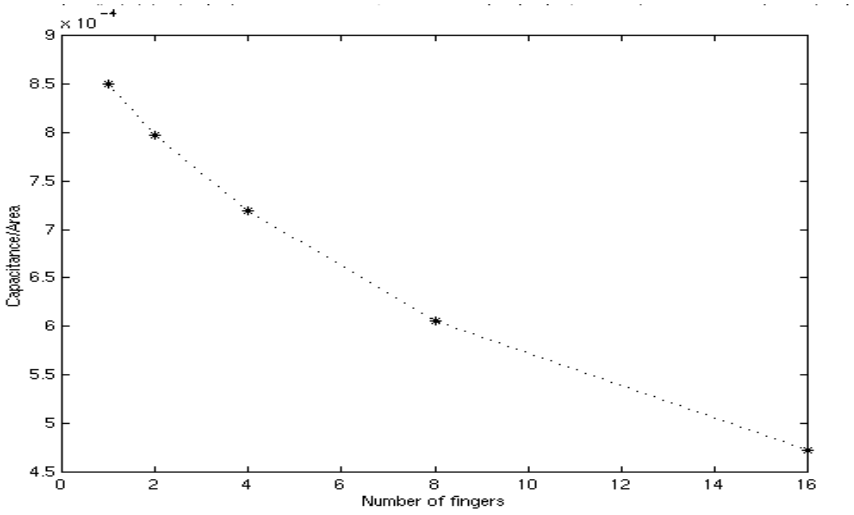

Figure IV-5: Capacitance per unit area Vs. Number of fingers.

The first plot shows a capacitance that increases linearly with the number of fingers. The obtained capacitance responds to:

$$C = 1..62\,rF + 0.0139 \cdot NrF$$

where N is the number of fingers. The factor reflecting the dependency on the number of fingers is about 70% higher than the approximately 8 nF/finger predicted by equation III-2. There could be many ways to explain this discrepancy. A major part could be due to inaccuracies during the fabrication process leading to a slight increase in the upper plate proportional to the number of edges.

In any case, the second plot shows that in terms of capacitance per area the fringing capacitance gained by fingering is not worth the extra chip area, and the capacitance per area decreases as the number of fingers increases.

IV.3 Simulated Results

We have simulated the MIM1, MIM2, MIM3 and MIM4 capacitors. The 16-finger device, MIM5 was not simulated because its complexity leads to a computational load that is too high.

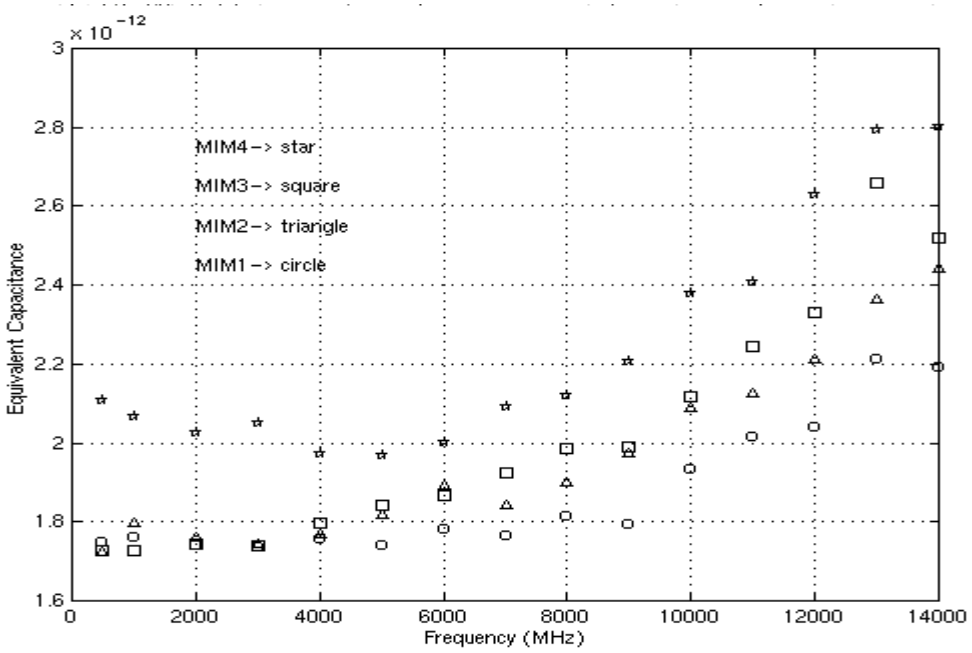

Figure IV-6: Equivalent Capacitance after de-embedding calculated from the Simulated S-parameters for different MIM Capacitors

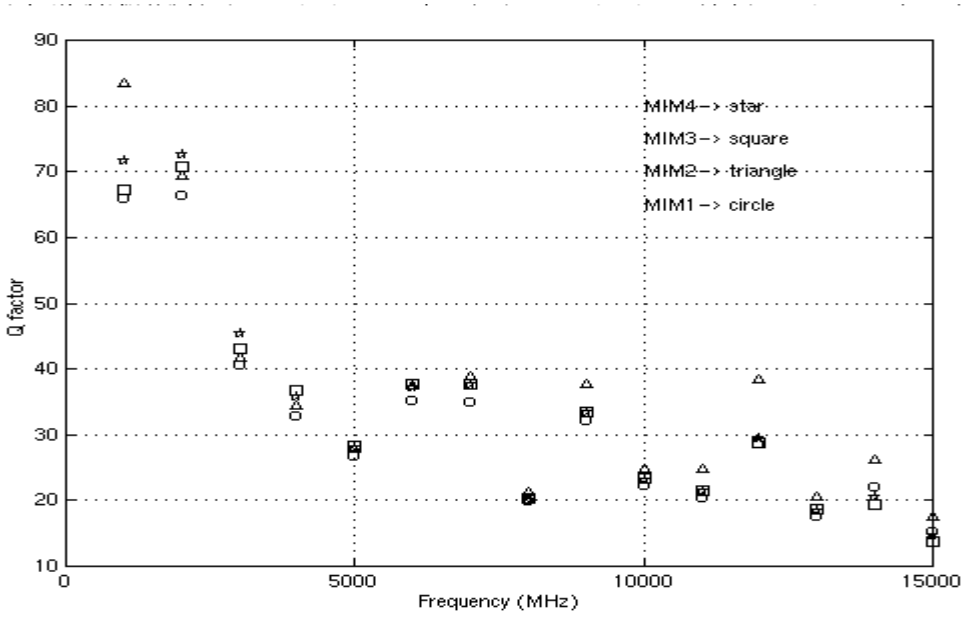

Figure IV-7: Quality Factor after de-embedding calculated from the Simulated S-parameters for different MIM Capacitors

Figure IV-6 shows the obtained equivalent capacitance as defined by Equation II-11. Qualitatively we see the same behavior found in the measurements. The bending of the line due to a parasitic inductance is less severe than in real measurements. That is because the de-embedding process described in section II.3 has eliminated the line inductance of the connecting lines, which caused most of this bending.

At low frequencies the values found for the 8-finger capacitor deviate from the expected behavior. These are simulation errors that appear at lower frequencies, as the structure becomes more complicated.

Table IV-2 in next page presents the capacitance and parasitic inductance computed. Again, the capacitance computed for the 8-finger structure is higher than expected even when we take into account the increase of capacitance due to the fringing fields.

Figure IV-7 displays the calculated Quality Factor. The values are widely spread because the real part of the impedance (B in the ABCD parameters) is very small, making the Q factor very sensitive to small errors. As in the measurements, as frequency goes up, the 2-fingered device seems to perform better in terms of its quality factor.

Fingers	C (ρF)	L (ρH)
1	1.72	15.2
2	1.75	20.0
4	1.75	23.3
8[2]	1.92 (1.99)	22.6 (17.7)

Table IV-2: Calculated Capacitance and Inductance for the simulated MIM Capacitors.

[2] To calculate this value the values of the equivalent capacitance at low frequencies have been ignored. Values between parenthesis are calculated using all data points.

V. Qualitative Study of the Electromagnetic Fields present in MIM Capacitors

One of the most important features of doing EM simulations is the added capability to study the shape and strength of the Electric and Magnetic fields induced inside the structure under study. Besides the capability to study non-existing devices, this is the principal reason to perform simulations.

It is very difficult, in many cases impossible, to directly measure these fields. Nevertheless being able to study them can provide a great amount of knowledge and understanding about the device. It can help explain its behavior, which can lead to better designs.

Of course, the limited computational power limits the accuracy of the calculated fields. As a result we cannot perform a precise quantitative analysis. However, we can recognize phenomena and qualitative behavioral trends.

Throughout this chapter we will use this capability to understand the differences between the different MIM structures considered. We will concentrate on the MIM1, MIM2 and MIM4 devices.

V.1 Fields in the MIM1 Capacitor at Different Frequencies.

First the fields in the (MIM1) single plate capacitor at different frequencies will be considered. Figure V-1 (page 42) shows a plot of the magnitude of the Electric and Magnetic field in a horizontal plane laying between the Metal-2 bottom plate and the TiN upper plate and parallel to both plates. Because this plane is very close to the upper plate, 10 nm, the magnetic field is closely related to the current density distribution on that upper plate. Therefore, we will use this magnetic field to study the current distribution.

The plots correspond to frequencies of 500 MHz, 2 GHz and 15 GHz. We choose the first and last frequencies because they represent the extreme cases, allowing us to easily detect high frequency effects. The intended operation frequency of these devices is close to 2 GHz, and therefore it is important to see how the devices behave at this frequency. All plots follow the same orientation as the layouts in Figure III-2. As the devices are symmetric, to reduce the computational load, only

half of them have been simulated. The plots correspond to the right half side of the devices as seen in Figure III-2. The magnitudes are given in arbitrary units[3].

The left column in Figure V-1 shows the Electric fields at different frequencies. As expected we encounter a high quite homogeneous electric field between both plates. The edges present some irregularities caused in most part by the limitations of the finite element solver. As the frequency increases we see that the field strength decreases. The reason for this is the inductance of the microstrip connecting the device. Ansoft's HFSS computes the fields while feeding a constant amount of energy into the system. At higher frequencies more of this energy is stored as magnetic energy as result of the parasitic inductance, leaving less for the capacitor. Note that the field strength is approximately proportional to the inverse of frequency.

The right column in Figure V-1 shows the magnetic fields, or, as we have said, it reflects the current distribution in the upper plate. There is also a contribution caused by the narrow paths connected to the bottom plate through via holes (see layout in Figure III-2).

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[3] Actually, units are V/m and Tesla. The simulator calculates the fields resulting of exciting the system with a signal of a constant power of 1 Watt.

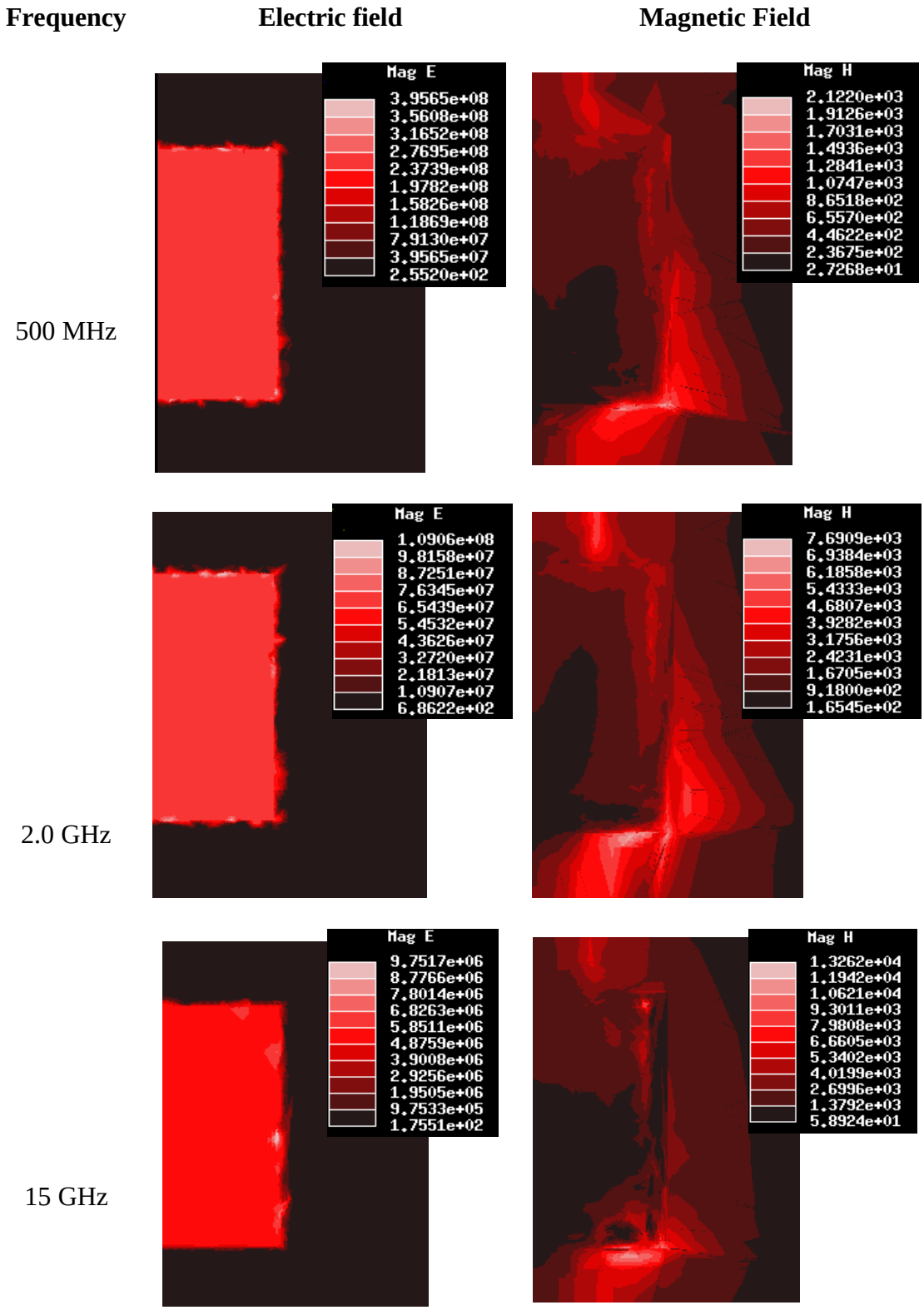


Figure V-1: Electric and Magnetic Fields between the MIM1 Capacitor plates (0.01 μm) at different frequencies. The magnitude of the magnetic field reflects the current distribution.

In the upper and lower part of each plot we can see the fields induced by the current distribution in the microstrip lines connecting the device Those fields are stronger near the edge of the microstrip. We can see how the skin effect [6] [7] pushes the current, in the horizontal direction, towards the edge of the microstrip. The same effect is responsible for the current density distribution in the capacitor plates. At higher frequencies current flow becomes more and more concentrated, accounting for induced magnetic fields that are stronger at a local level.

At 15 GHz it looks as if relatively little current is getting into the capacitor itself. While at lower frequencies we can clearly see the field induced by the current flowing through the narrow side paths to the bottom capacitor, at 15 GHz very little current seems to be going through those paths. The high parasitic inductance of those paths could cause this effect.

V.2 Comparison of Different Layouts at 500 MHz.

In this section we will compare the fields for the three devices considered at a relatively low frequency of 500 MHz. This will be useful especially when comparing with the corresponding fields at 15 GHz.

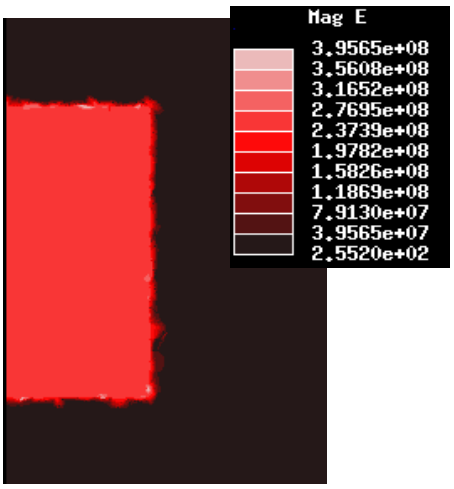
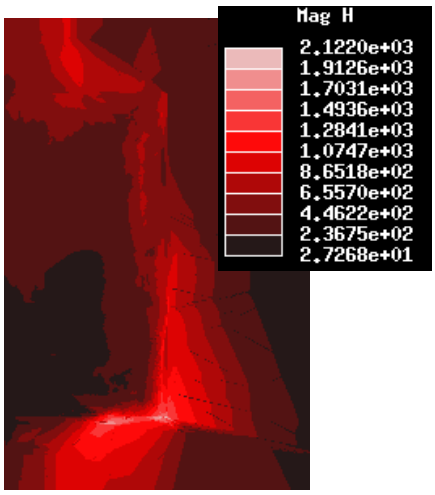
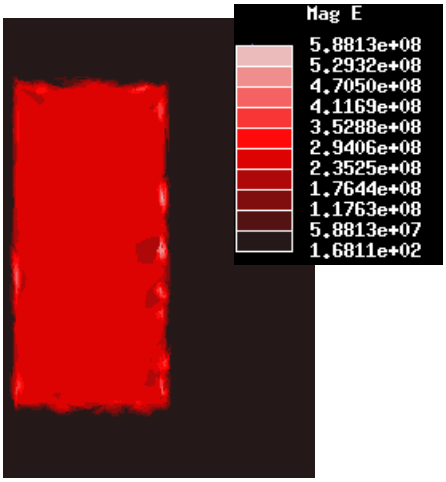
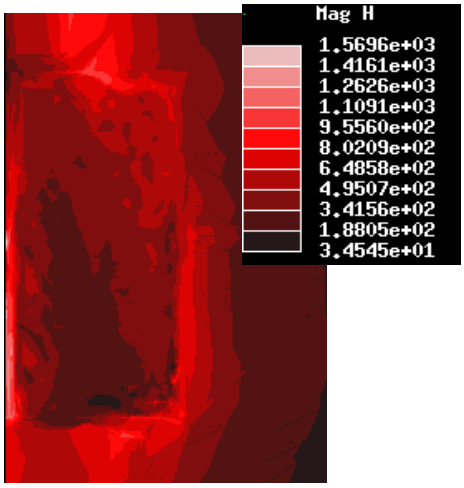
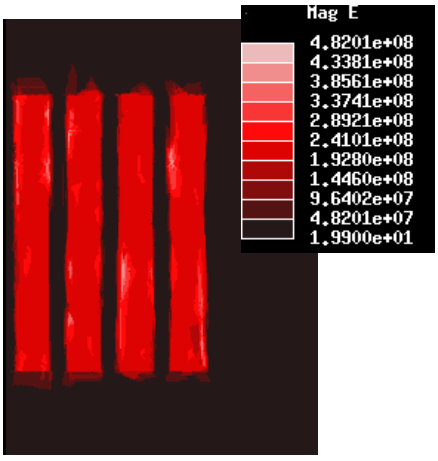
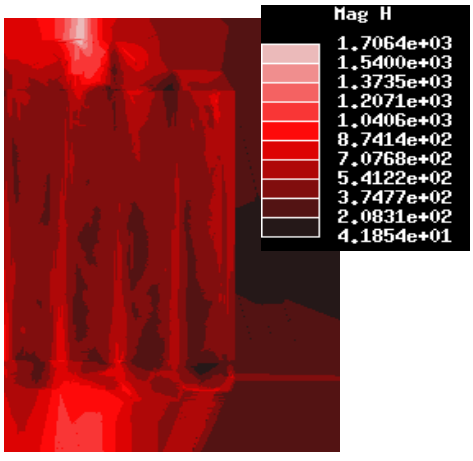
Device	Electric field	Magnetic Field
MIM1 (1 finger)		
MIM2 (2 finger)		
MIM4 (8 finger)		

Figure V-2: Electric and Magnetic Fields between the MIM1, MIM2 and MIM4 Capacitor plates at 500 MHz

The first thing we can appreciate looking at the electric fields is the existence of unexpected artifacts (darker or lighter spots). These artifacts are due to the finite element solver, and we see that the more complex devices present more of these artifacts.

Due to different color scales it is difficult to compare the magnitudes of the fields. We expect the fields to become weaker as the number of finger decreases. The reason is that we have a larger capacitance storing about the same amount of energy, so, the energy is distributed over a larger area and, therefore, the fields should be smaller. However, the differences should be small, and this effect cannot be confirmed.

Looking at the induced magnetic fields we see how fingering the upper plate and adding more paths to connect the bottom plate results in spreading the current. This reduces both the series resistance and the parasitic inductance of the device.

V.3 Comparison of Different Layouts at 15 GHz.

Now we take a look at the fields at the highest frequency simulated, 15 GHz (figure V-3), well beyond the intended operating frequency (a couple of gigahertz).

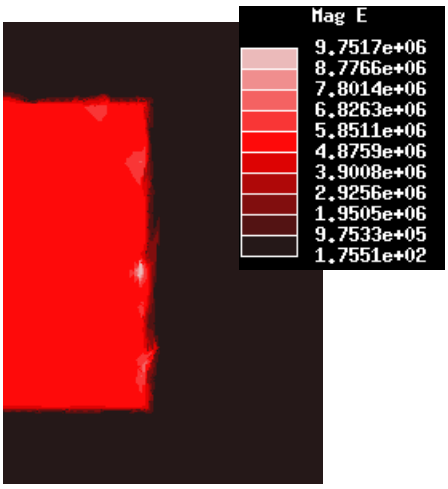
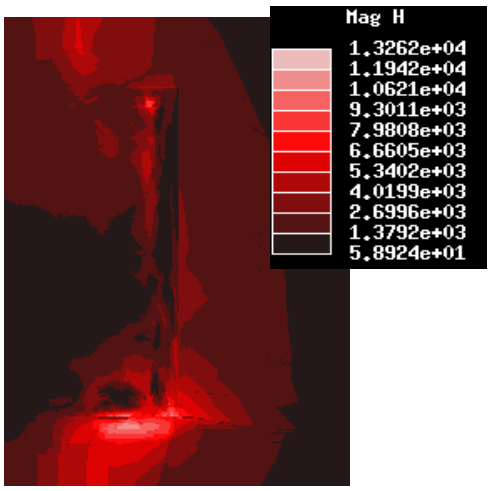
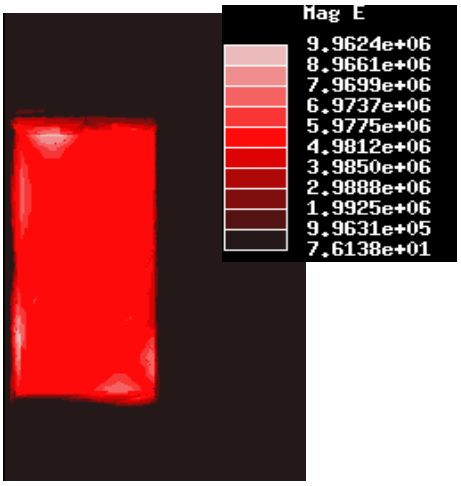
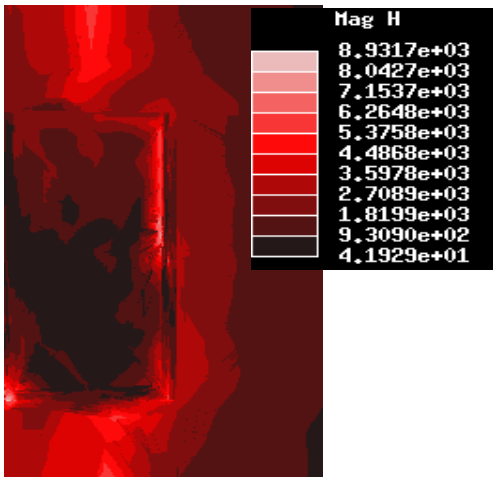
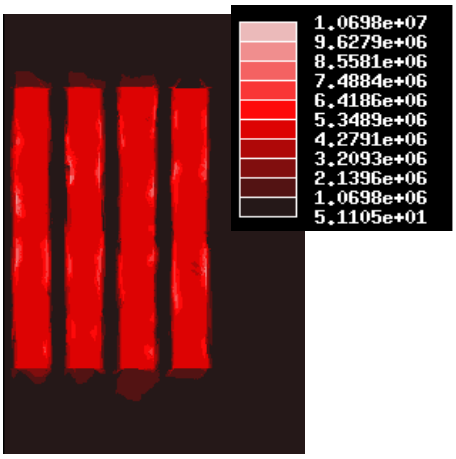
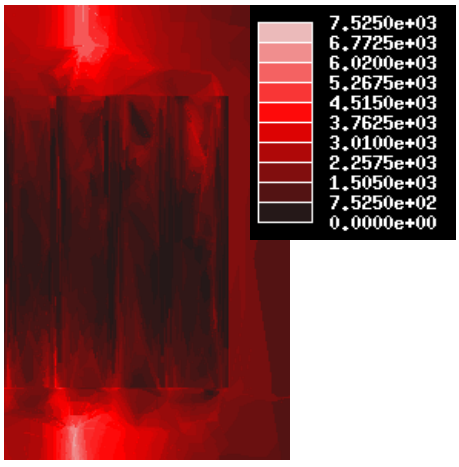
Device	Electric field	Magnetic Field
MIM1 (1 finger)		
MIM2 (2 finger)		
MIM4 (8 finger)		

Figure V-3: Electric and Magnetic Fields between the MIM1, MIM2 and MIM4 Capacitor plates at 15 GHz

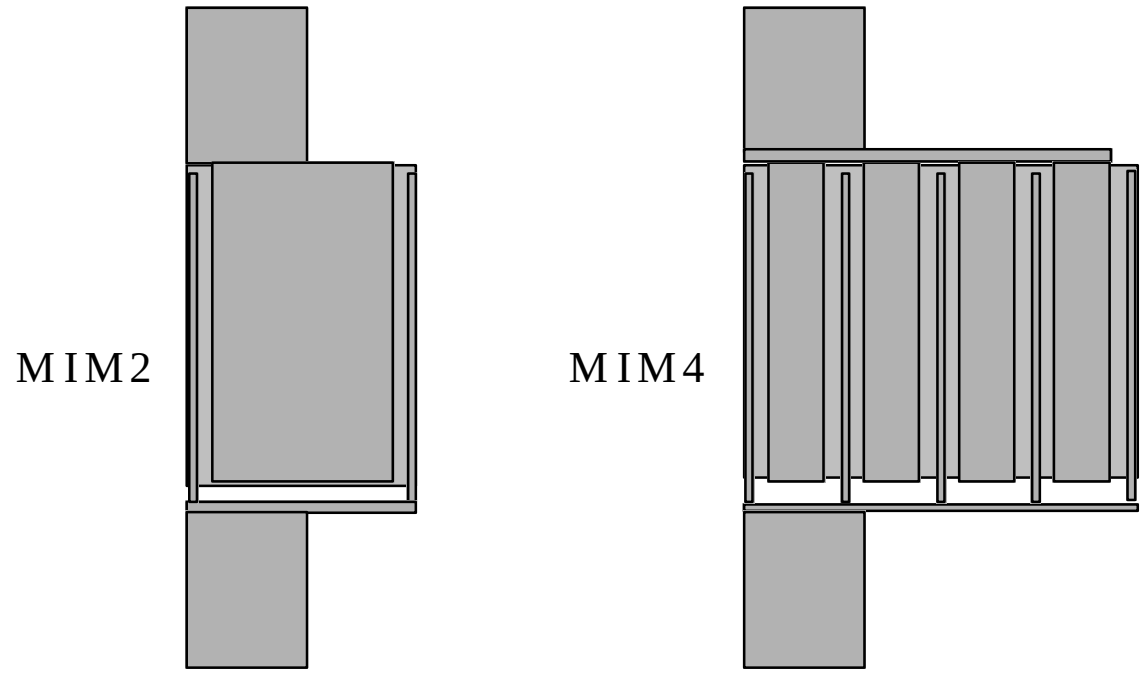


Figure V-4: Detail of the simulated half layout of the MIM2 and MIM4 Capacitor

Upon carefully studying the electric fields associated to MIM4, the 8-finger device, we observe that they are lower than the fields in the other devices. In some sense there must be less current getting into the device. That would point to a mismatch, or an additional mismatch to be more precise, between the microstrip and the capacitor.

The magnetic fields reflecting the current distribution seem to confirm this situation. We observe that the fields present inside the 8-finger capacitor are very weak in comparison to those in the other devices. In particular it seems that the outer narrow paths to the bottom plate are carrying very little current. For the 2-finger case we see a similar effect, but it is the middle path that seems to be carrying little current.

Summarizing, in comparison to the field distributions at 500 MHz, the current densities are now less uniformly distributed. Ideally we would like to have a uniform distribution of the current among all the fingers, but that is not happening. As a result, the parasitic inductance and the series resistance will be higher than if the current distribution was uniform.

Figure V-4 schematically shows the simulated half MIM2 and MIM4 layouts. Considering the upper plate, we can see that, although fingering can be beneficial in some ways, the outer fingers are poorly connected to the microstrip. The narrow horizontal path connecting the fingers can act as a bottleneck that limits the performance of the device.

For the lower plate adding the extra paths should only be beneficial, but in the case of the outer fingers a poor connection limits the improvement.

Finally, because of the skin effect the current coming in through the connecting microstrip concentrates in the outer edge (right edge in figure V-4), and thus the middle connecting path hardly *sees* this current.

V.4 Comparison of Different Layouts at 2 GHz.

Now we will examine the fields at 2 GHz (Figure V-5), which is a frequency close to the intended operating point of these devices.

As in the previous cases we cannot learn too much from the electric fields, which display in all cases reasonably well behaving capacitors. Much more can be learnt from the magnetic fields.

Looking at the 2-finger device we see clearly how part of the current going into the plate goes close to the inner edge of the plate. We know that the skin effect will push the current towards the edges of the plate, and by adding more edges we are gaining alternative paths. This should decrease both the parasitic inductance and series resistance. On the other hand we see that the current flowing close to the center of the device is much smaller than the current along the outer edge.

If we now look at the current flowing through the narrow paths connecting the lower plate we see that in the 2-finger device case almost all the current is going through the outer path, making the center path of little use. For the 8-finger device we see that all the different paths are carrying different current. The picture clearly shows how paths that are closer to be a prolongation of the edge of the microstrip carry the highest current, whereas the center path and the outer path hardly conduct current.

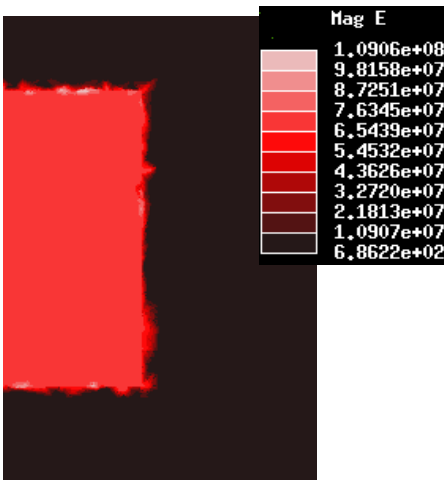
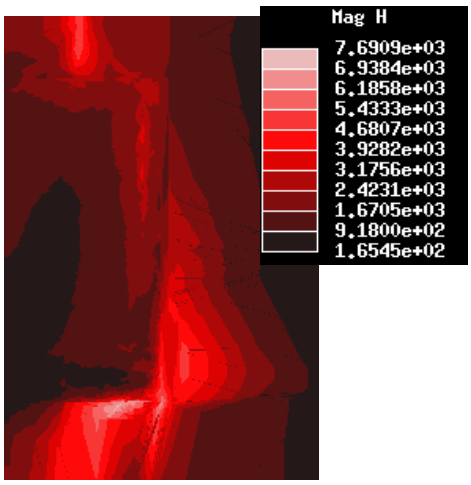
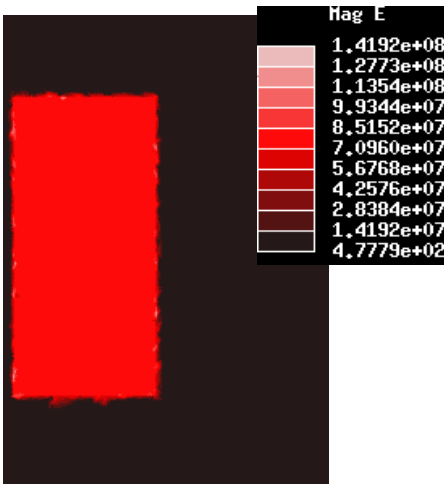
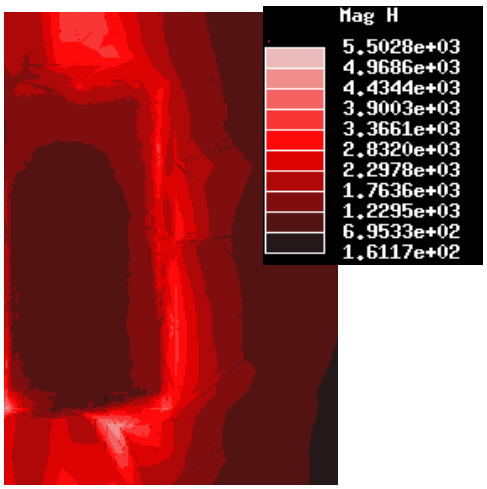
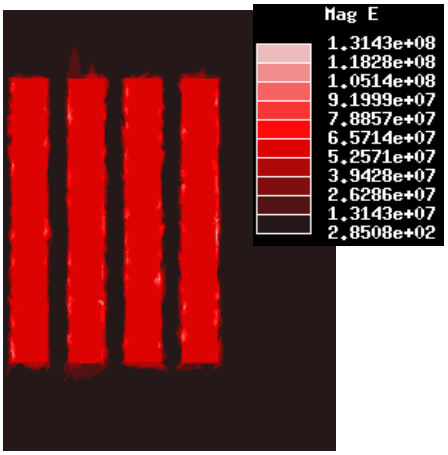
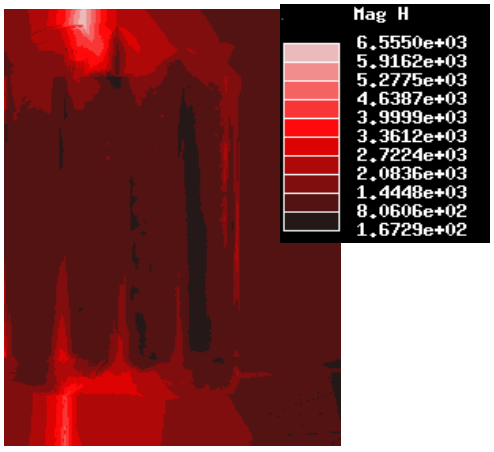
Device	Electric field	Magnetic Field
MIM1 (1 finger)		
MIM2 (2 finger)		
MIM4 (8 finger)		

Figure V-5: Electric and Magnetic Fields between the MIM1, MIM2 and MIM4 Capacitor plates at 2 GHz.

Another interesting feature is the strength of the induced fields outside the device. As the capacitor is a part of an integrated circuit along with other active or passive devices, the strength and reach of these *spillover* fields will determine how close the designer can place other devices that could be sensitive to these fields. Having large current densities in the outer part of the device, as in the case of the MIM1 Capacitor and to a lesser degree for the MIM2 Capacitor will increase the effective area used by those devices.

Our hypothesis is that the connection of the device to the microstrip has an important influence on the current distribution inside the device. In order to get a more optimal, uniform, current distribution, either the connection has to be modified or the device has to be designed taking into account the connection to the microstrip. For example, following this last approach we would eliminate the central and the outer paths, as they are occupying space while driving no current.

V.5 A modified MIM4 Capacitor

In order to test the importance of the connection of the device to the microstrip we have simulated a modified MIM4 Capacitor. Figure V-6 shows the simple modification introduced. We suggested in previous sections that the narrow horizontal (as seen in the pictures) paths connecting the fingers in the multi-finger

devices could be acting as a bottleneck that severely limits the effect of having that fingered structure.

To reduce this effect, in our alternative design we have substituted those narrow paths by a triangular structure. By doing so we hope to obtain a more uniform current density distribution in the device.

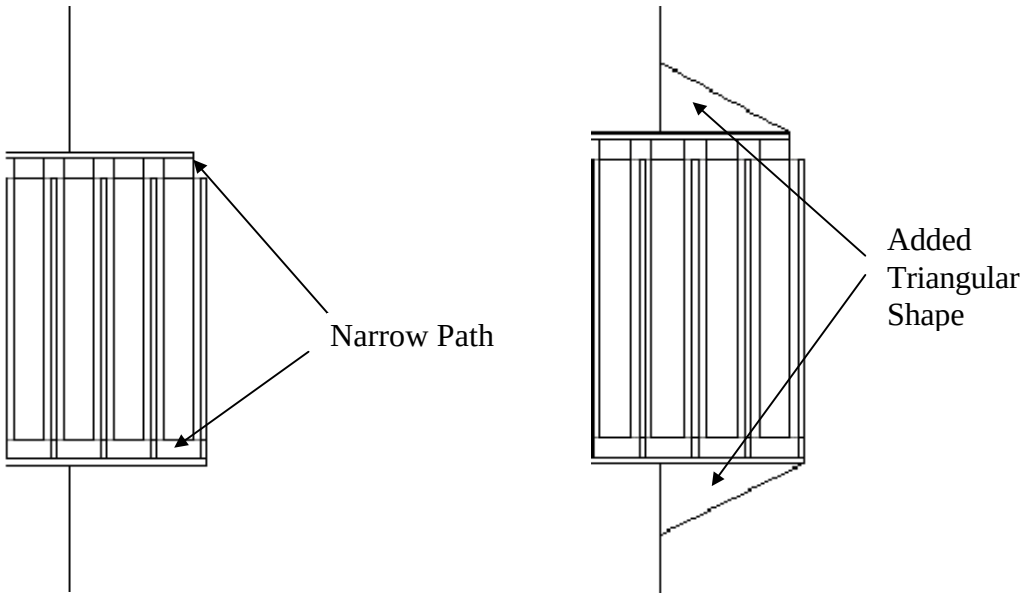


Figure V-6: Original and modified MIM4 layout. The triangular shapes should reduce the bottleneck effect of the horizontal (narrow) paths connecting the fingers in the original designs.

Figure V-7 shows the induced magnetic fields together with the original fields. We see how the current distribution has changed. In general, we obtain a more homogeneous distribution, which was one of the objectives of this modification. We also see that current densities tend to be displaced toward the outer part of the device, as a result of having an easier *route* to the outer fingers and outer paths.

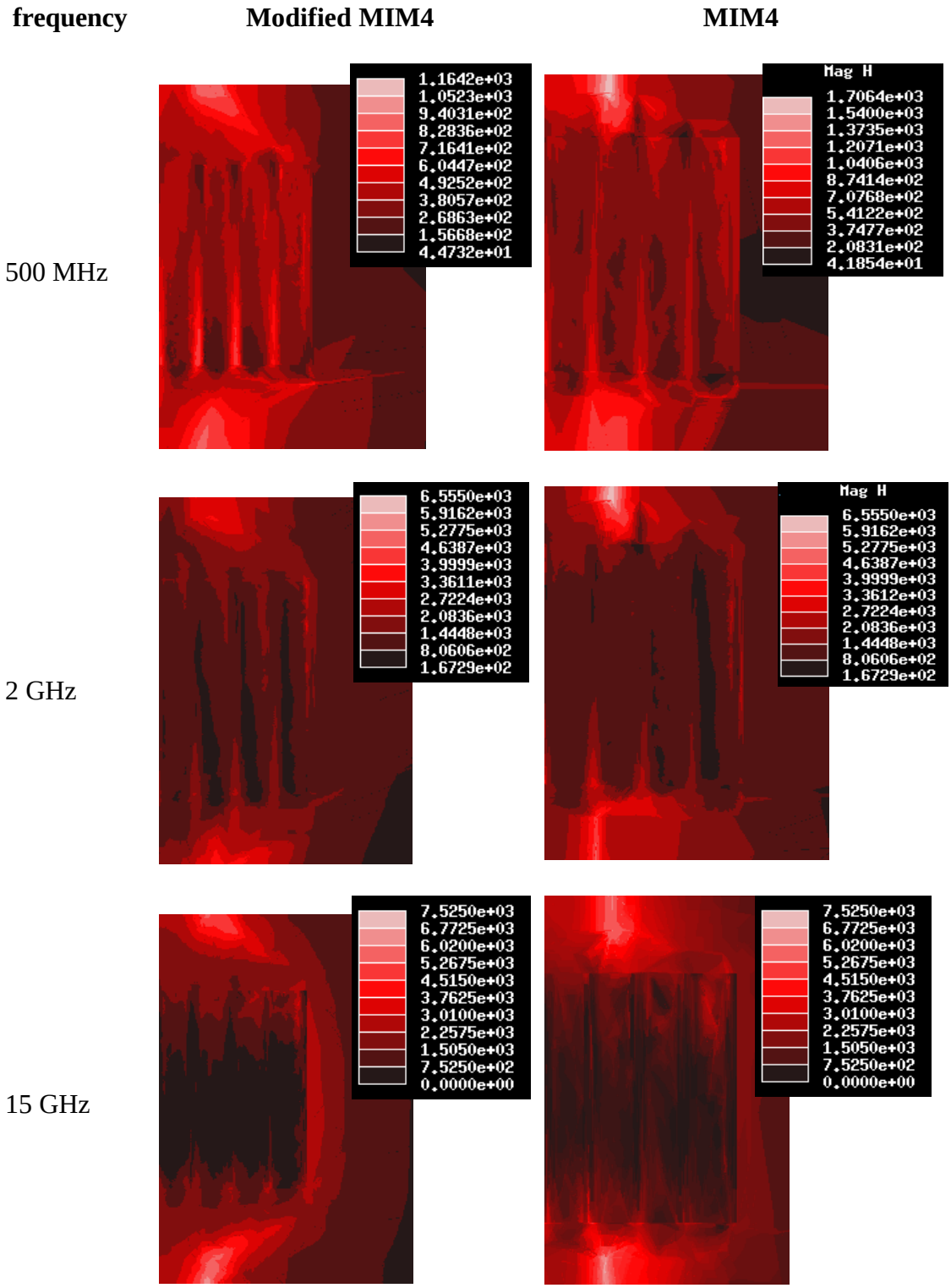


Figure V-7: Magnetic Fields between the Modified and original MIM4 Capacitor plates at different frequencies.

At 15 GHz we see how most of the current going to the bottom plate is going through the outer path. In that case the modification has reversed the original problem. At 2 GHz the pictures suggest an easier flow of current into the device.

We may conclude that there must be an optimal shape, an optimal way to connect the device to the microstrip, which would lead to an optimal (as uniform as possible) current distribution. This optimal shape is not general but frequency dependent.

The performance of the MIM capacitors under study is not very sensitive to how homogeneously the current is distributed. Despite the non-homogeneous current distribution, the electric field remains very uniform. In fact, non-uniformity of that electric field would necessarily imply a voltage difference between different points in the capacitor (on a same plate). This would lead to a compensating current.

However, there are other fingered devices that could be much more sensitive to the current distribution. Examples are multi-finger FETs [8] or HBTs. For example, we have seen that at high frequencies the middle path hardly is carrying any current. That could dramatically affect the behavior of an HBT with an uneven number of fingers. For such a device there is a finger left in the middle, and that middle finger will be isolated from the edges of the connecting microstrip.

To finish this section I would comment that the modified MIM4 Capacitor leads to a *better* simulation than for the original device. Better in the sense that the calculated parameters have a smoother frequency response and that the values for the capacitance, 1,80 ρF, and for the parasitic inductance, 29.5 pH are closer to what could be expected (see Table IV-1 and Table IV-2). This is reasonable because a structure with smoother fields will be easier to simulate (see Appendix I). However, despite being reasonable, it clearly shows some limitations of HFSS.

VI. Conclusions and Future Work

We have used a Full 3D Electromagnetic Field Simulation technique as a complement to measurements in studying MIM Capacitors at high frequencies. Both the MIM Capacitors and the simulation technique itself was the object of this research project.

VI.1 The MIM Capacitors

One of the points of interest was to see the capacitance gain due to the fringing capacitance when fingering the upper capacitor plate. We have found that the capacitance gain was higher than expected, but insufficient to increase the effective capacitance per unit area. It remains to be studied if smaller spacing between the

plates would lead to an improved capacitance per area, which will be possible as new processing techniques allow smaller dimensions in the layouts.

Another purpose of the novel structures that were studied was to reduce the parasitic circuit elements associated with the capacitors. Regarding the parasitic inductance the measurements were inconclusive. It is our belief that the dominant line inductance is masking the parasitic inductance. Measurements should be done very carefully and on-wafer calibration would be recommended.

Simulations suggest a growing inductance as we add more fingers. This trend was broken for the 8-finger device, but we recover it with the modified structure.

Measurements clearly show that fingering the structure reduces the series resistance, although the effect becomes less significant and even reverses beyond a certain number of fingers.

In general, we have seen that, for a few gigahertz, adding more fingers is beneficial as the Quality factor improves. This improvement, though, does not come without a cost since the capacitance per area worsens. The main reason for this improvement is the lower resistance of the connection to the lower plate. Then, over-fingering the structure is detrimental because the connection to the upper plate becomes worse.

At higher frequencies the picture becomes more evolved. As with the skin effect the higher induced magnetic fields shape the current distribution. On one hand this increases the series resistance directly. However, it also reduces the current flowing into certain parts of the structure. Similar effects have been reported in other fingered devices, which makes the search for an optimal geometry, in electromagnetic sense, an important goal.

VI.2 The 3D Electromagnetic Field Simulation Technique

3D Electromagnetic Field Simulation has proved to be a useful tool to study passive elements for integrated circuits. It demonstrates a potential that could also be of use for the evaluation of active components. This will become possible as the next generation of 3D EM simulators will include models for semi-conducting materials.

The simulation results are in consistent agreement with the results obtained by measuring the device, but with some added abilities, like being able to examine the induced EM fields. This has been proven to be of use to identify phenomena and to suggest ways to improve the performance of the devices.

Nevertheless, at this point, with our available computing resources, the simulation technique is still relatively slow. For each device and frequency point the simulation can take several hours, and even then the results are not as accurate as desired.

A problem we have been dealing with throughout our work is that the software used is not designed for IC applications, thus creating additional difficulties in handling the problem. These difficulties are not inherent to the method; instead they are a result of its implementation. Software designed specifically for IC probably would result in much more accurate simulations. Later in this section several ideas in this direction are proposed.

It is our belief that the IC industry will be in need of reliable and easy-to-use simulation tools, especially as frequencies go up and systems become further integrated.

VI.3 Lines Future of Work

We divide our future lines of work in two parts. First we identify work to do regarding the Capacitors, or IC devices in general:

1. The geometry of the device has to be optimized in terms of the associated Electromagnetic Fields. The shape of the connection between the device and the feeding microstrip has to be carefully studied. In addition, the distance between fingers should be optimized, where a non-uniform pitch could be of interest.
2. Possibilities to improve the capacitance per area should be studied. It has to be determined if by reducing the spacing between fingers the extra fringing capacitance can at some point compensate the loss of *parallel plate capacitance*.
3. More accurate measurements need to be made, with carefully on-wafer calibration to be able to completely eliminate effect related to the connecting lines. This is necessary to be able to find an accurate equivalent model for our devices.

The second set of future work lines is related to the simulation tool itself. Although we have been using a commercial tool, creating a new tool is not unthinkable. It could be possible to start collaborations with EM Field Simulation software providers to improve the available software to meet the need of the IC designer. Along this line of thought we have several ideas:

1. Implement an automatic and easy-to-use translation stage that would allow us to generate the simulation model directly from the layouts and process specifications.
2. Introduce standard signal sources. One of the difficult points when creating a simulation was to feed the signal into the system. When dealing with IC circuit

design we will encounter very specific structures, like the microstrip. An already optimized set of standard ports would result in better simulations at a lower computational cost.

3. Design a new *mesher* specifically suited for IC devices modeling. Probably the most critical and difficult part of the finite elements method is finding the right mesh (see Appendix 1). However, IC-related models have some characteristics that suggest that a specific algorithm designed to create this mesh would be very beneficial. One of these features is that the devices are very planar. The second is that we can allow a less accurate solution far away from the device.

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APPENDIX I: The Finite Element Method solution of the 3D Electromagnetic Fields.

IN this appendix we will briefly cover the main features of the used simulation software: Ansoft's HFSS. Although we are simply users of this software and could work with it without knowing anything about its implementation, it is important to know how the software handles the problem. This will help us understand its capabilities and limitations.

A1.1 The Finite Element Method

Finite element methods divide the problem space into a large number of smaller regions, representing the field in each sub-region (element) with a local function. In HFSS these elements are tetrahedra. The set of all these tetrahedra is referred to as the Finite Element Mesh.

To represent the vector field quantities (H field, E field or related quantities), the method basically stores the values of these fields at the vertices of each tetrahedron. The fields inside each mesh element are interpolated from the values at the vertices.

By representing the fields in this way the Maxwell equations can be approximated and converted into (large) matrix equations that can be solved using traditional numerical methods.

The accuracy of the solution so obtained is dependent on the relative size of the tetrahedra. These tetrahedra have to be small in the sense that the field values can be well interpolated inside each element. Obviously, reducing the size of each element will reduce the interpolation error and, therefore, improve the solution. However, at the same time it will increase the size of the matrix equation to be solved, which is limited by computational limits.

To achieve an optimal compromise between size and accuracy HFSS uses an iterative process in which the mesh is automatically refined in critical regions.

A1.2 Implementation of the process in HFSS

Figure A1-1 shows a flowchart of the simulation process. It starts creating a first coarse mesh. Then the excitation current pattern at the ports where through the signal will be fed to the system is computed. This excitation signal is tested by

comparing $\nabla \times \vec{H}$ to $\vec{E}$ and $\nabla \times \vec{E}$ to $\vec{H}$. If the result of this comparison is not satisfactory the mesh is refined at the ports and the process is repeated.

The method considers each port to be the end of a waveguide with the port shape as

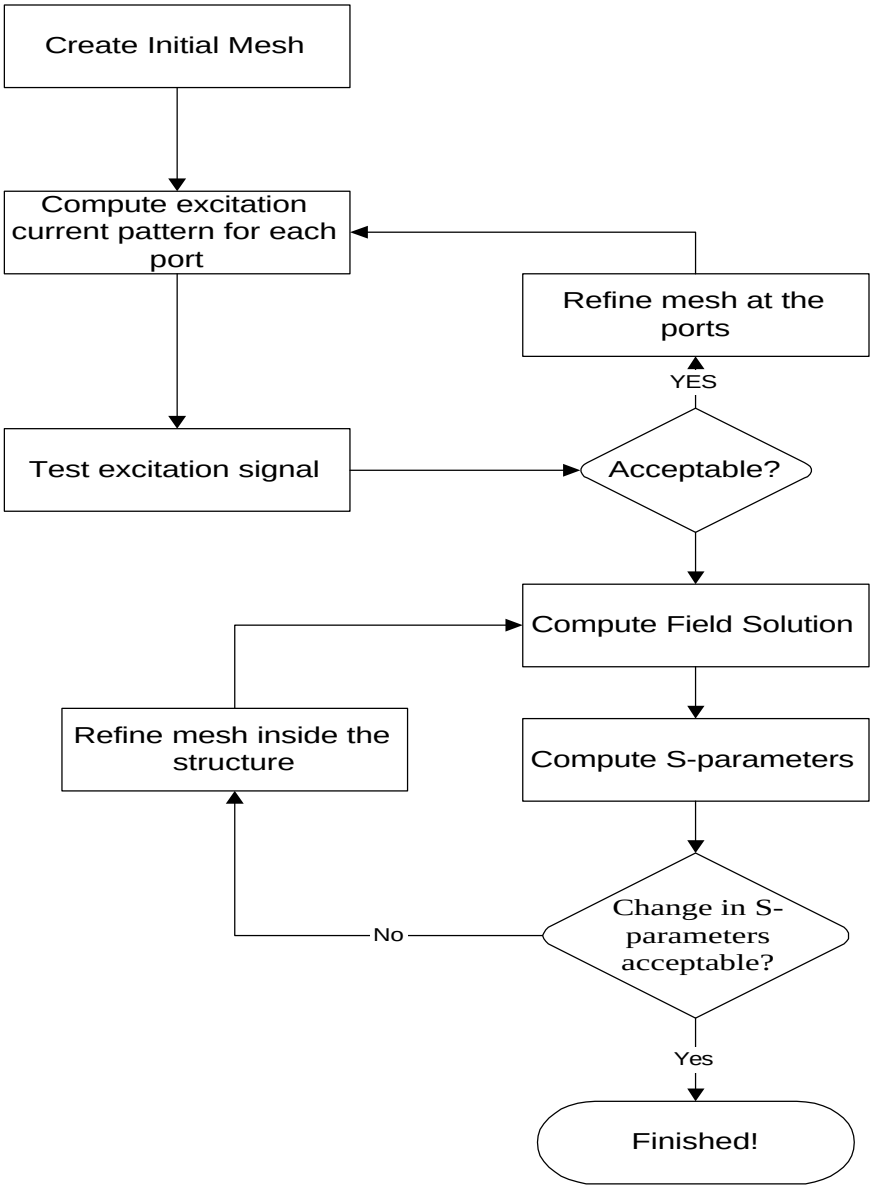

Figure A1-1: Flowchart of the solution process in HFSS

cross section. It solves the wave equation

$$\nabla \times \left(\frac{1}{m_r} \nabla \times \vec{E}(x,y) \right) - k_o{}^2 e_r \vec{E}(x,y) = 0 \qquad \text{(A1-1)}$$

The solution of the 2D wave equation at the port serves as boundary condition for the 3D problem.

Once the current distributions at the ports are acceptable, a similar loop is entered to solve the fields. Now the wave equation is

$$\nabla \times \left(\frac{1}{m_r} \nabla \times \vec{E}(x,y,z) \right) - k_o{}^2 e_r \vec{E}(x,y,z) = 0 \qquad \text{(A1-2)}$$

where all the values are complex values and k_0 is equal to $w\sqrt{m_o \cdot e_o}$, and the resulting real electric field will be equal to

$$\vec{E}(x,y,z,t) = \Re\left[\vec{E}(x,y,z) \cdot e^{iwt} \right] \qquad \text{(A1-3)}$$

Each iteration the program refines the mesh at critical areas. A good meshing algorithm is critical to achieve a good solution. A possible problem of HFSS when applied to IC structures is that the meshing algorithm is general and not specifically designed to deal with very planar geometries.

APPENDIX II: Implementation of the de-embedding process.

For future use or reference we include some of the MATLAB routines written to implement.

A2.1 Extraction of the ABCD-Parameters of the Input Port

Several routines implement the process. Assuming some basic knowledge about MATLAB the program is self-explained.

The most important routine, listed below, calculates the ABCD parameters for the input/output Port minimizing II-9.

```
function [ABCD,Z]=dembed1(Ac,Az,Z,out)

%  function ABCD=dembed1(Ac,Az,Z,out)
%
%  Az and Ac are ABCD parameters writen as a vector
[A,B,C,D]
%  This function calculates de ABCD parameters for a 2-
port P %knowing
%  the ABCD parameters for a cascade of two times P and
those %fos a cascade
%  "P Q P" where Z is of the form
%
%       -----ZZZ-----
%
%
%       -------------
```

```
%
%  With Z a known impedance
%
%  if out=1 then the function displays some information,
for %debugging purposes:)
%
%  By Paco Lopez Dekker, UCI 8/4/98
%

%Computation of A and C
A=-sqrt((Az(2)-Ac(2))/Z);
C=-sqrt((Az(3)-Ac(3))/Z);

%Computation of C and D;
B=Ac(2)/(2*A);
D=(1+B*C)/A;
A=A;
var2opt=[real(A),imag(A),real(B),imag(B),real(C),imag(C),
...
real(Ac(1)+Ac(4))/2,imag(Ac(1)+Ac(4))/2,real(Ac(2)),imag(
Ac(2)),real(Ac(3)),imag(Ac(3)),...
real(Az(1)+Az(4))/2,imag(Az(1)+Az(4))/2,real(Az(2)),imag(
Az(2)),real(Az(3)),imag(Az(3)),...
  real(Z),imag(Z)]';
  var2opt'

%Now we check the answers...
if(out==1),
disp('So, you want to see some data.....?');
ABCD=[A B C D];

Fabcd_err2(var2opt)

Fabcd_grad_opt2(var2opt)
end;

%Steepest descent minimization of the error function.
%What do we want to optimize??
mask=[ones(1,6),zeros(1,12),0,0]';
parm=[0,0,0,100];
parmc=[parm,2];

%[optvar, fabcd_err, df,
nit,xpts,fpts]=steepest('Fabcd_err2','Fabcd_grad_opt2',va
r2opt,1,parm,mask);
[optvar, fabcd_err, df,
nit,xpts,fpts]=cgrad_fr('Fabcd_err2','Fabcd_grad_opt2',va
r2opt,parmc,mask);
nit


if(0),
  %Is it really a minimum? Lets see som graph's...
  for k=[1,2,3,4,5,6,19,20],
     sav=optvar(k);
```

```
      qq=[];
      for q=(sav-1):0.1:(sav+1),
        optvar(k)=q;
        qq=[qq Fabcd_err2(optvar)];
      end
      figure(k);
      plot((sav-1):0.1:(sav+1),qq);
      optvar(k)=sav;
    end;
  end
```

```
A=optvar(1)+i*optvar(2);
B=optvar(3)+i*optvar(4);
C=optvar(5)+i*optvar(6);
D=(1+B*C)/A;
Z=optvar(19)+i*optvar(20)
fabcd_err
Fabcd_grad_opt(optvar)
ABCD=[A B C D];
```

Table A2-1: Computation of the Port's ABCD-Parameters.

The second routine uses the previous one to compute the port's ABCD-Parameters for a list. The functions **Fabcd_err2**, **Fabcd_grad_opt2** implement the function in Equation II-9 and the gradient of this function. The functions where obtained using MAPLE.

The function **cgrad_fr** implements the Fletcher-Reeves Conjugate Gradients Method.

The function **dembed2** uses **dembed1** to automate the process for a set of data at different frequencies.

A2.2 De-embedding of the ABCD parameters for the DUT

In Table A2-2 we have listed the routine that implements the de-embedding of the ABCD-parameters for the Device Under Test (DUT), using the result of function **dembed2.**

```
function Fao=dembed3(Fap,Fat,Z,out)

%  function Fao=dembed3(Fap,Fat,Z,out)
%
%  Calculates de ABCD matrix for the device.
%  Inputs:
%  Fac and Faz are ABCD parameters list as produced by
S2ABCDlist
%  Z is a starting impedance
%  Outputs:
%  FP is a ABCD parameters list containing the ABCD
parameters of the iiput
%  port.
%  FZ is a list containing the calculated impedances
%
%lc &lz are the current positions in both input lists
lp=1;
lpp=1;
ltt=1;
lt=1;
[Lp,aux]=size(Fap);
[Lt,aux]=size(Fat);
Fap=[Fap;0 0 0 0 0];
Fat=[Fat;0 0 0 0 0];

not_ended=1;
Fao=[];
FZ=[];

while(not_ended),
  F=Fap(lp,1)
  lpp=lp;
  while(F==Fap(lp+1,1))'
    lpp=lpp+1; %Just in case this frequency is repeated
```

```
    end
    %look for F in Faz
    while(F>Fat(lt,1) & lt<=Lt),
      lt=lt+1;
    end
    if(lt>Lt),
      break;
    end
    if(F==Fat(lt,1)),
      %BINGO!!!!
      ltt=lt;
      while(F==Fat(ltt+1,1)),
        ltt=ltt+1; %Just in case this frequency is repeated
      end
      Ap=mean(Fap(lp:lpp,2:5),1);
      At=mean(Fat(lt:ltt,2:5),1);
      %Now THE REAL WORK!!!!
      P=[Ap(1) Ap(2);Ap(3) Ap(4)];
      Q=[Ap(4) Ap(2);Ap(3) Ap(1)];
      S=inv(P)*[At(1) At(2);At(3) At(4)]*inv(Q);
      Fao=[Fao; F S(1,1) S(1,2) S(2,1) S(2,2)];
      %FZ=[FZ; F Z];
    end
    lp=lpp+1;
    lt=ltt+1;
    if(lp>Lp | lt>Lt),
      not_ended=0;
    end
  end;
```

Table A2-2: De-embedding of the DUT's ABCD-Parameters